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(12) **United States Patent**
Miyashita

(10) **Patent No.: US 9,093,553 B2**
(45) **Date of Patent: Jul. 28, 2015**

(54) **METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE INCLUDING TRENCH EMBEDDED WITH SEMICONDUCTOR LAYER**

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(73) Assignee: **FUJITSU SEMICONDUCTOR LIMITED**, Yokohama (JP)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **14/258,249**

(22) Filed: **Apr. 22, 2014**

(65) **Prior Publication Data**

US 2014/0227838 A1 Aug. 14, 2014

Related U.S. Application Data

(62) Division of application No. 12/544,810, filed on Aug. 20, 2009, now Pat. No. 8,741,711.

(30) **Foreign Application Priority Data**

Sep. 22, 2008 (JP) 2008-243309

(51) **Int. Cl.**
H01L 21/8238 (2006.01)
H01L 29/78 (2006.01)

(52) **U.S. Cl.**
CPC ***H01L 21/8238*** (2013.01); ***H01L 21/823807*** (2013.01); ***H01L 21/823814*** (2013.01); ***H01L 29/7848*** (2013.01); *H01L 2924/0002* (2013.01)

(58) **Field of Classification Search**
CPC H01L 2924/0002; H01L 21/823807; H01L 21/823814; H01L 2924/00; H01L 29/7848; H01L 21/8238
USPC 438/199, 299, 119, 229–232; 257/E21.334
See application file for complete search history.

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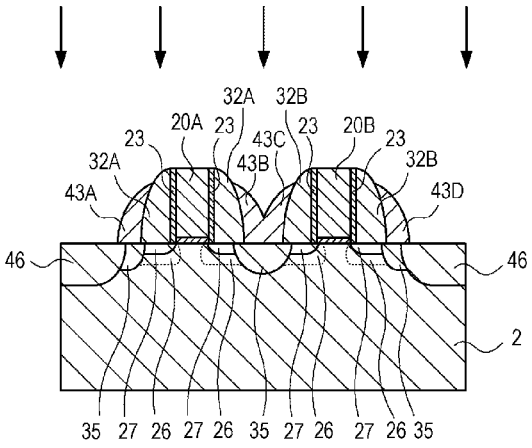
Primary Examiner — Duy T Nguyen
(74) *Attorney, Agent, or Firm* — Westerman, Hattori, Daniels & Adrian, LLP

(57) **ABSTRACT**

A method of manufacturing a semiconductor device which includes forming first and second gate patterns, forming first and second sidewall spacers on sidewalls of the first and second gate patterns respectively, implanting a first impurity into the semiconductor substrate, forming a third sidewall spacer on the first sidewall spacer and a fourth sidewall spacer on the second sidewall spacer in such a manner that the third sidewall spacer is in contact with the fourth sidewall spacer between the first and second gate patterns, implanting a second impurity into the semiconductor substrate, and removing the third and the fourth sidewall spacers.

4 Claims, 17 Drawing Sheets



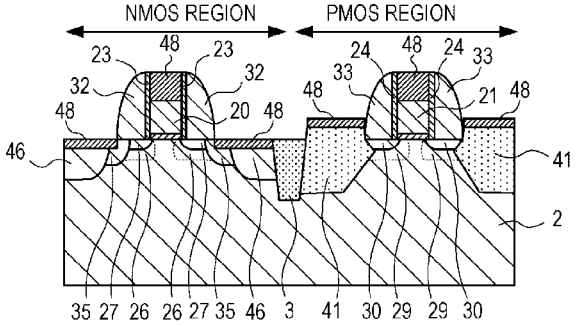


FIG. 1A

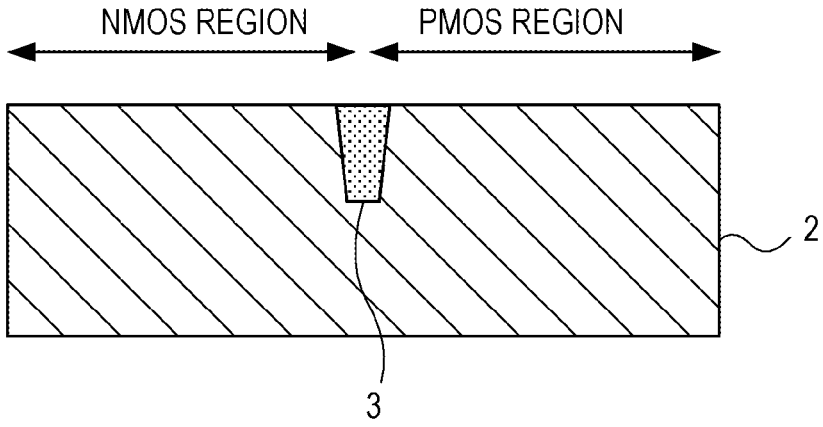


FIG. 1B

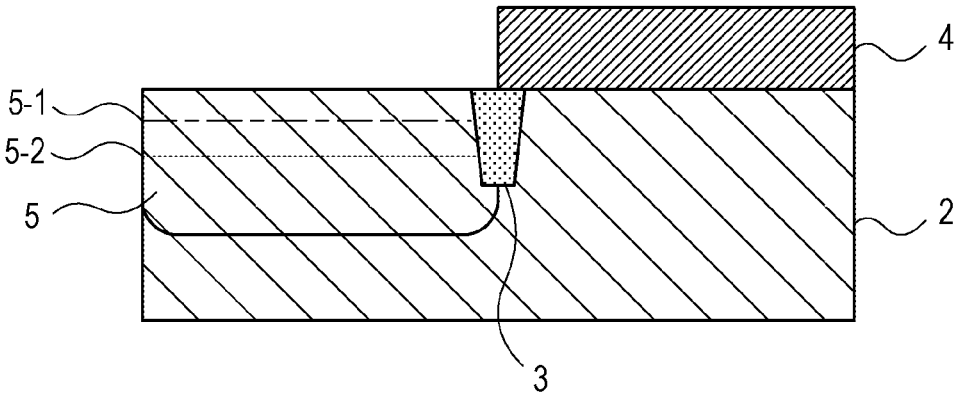


FIG. 1C

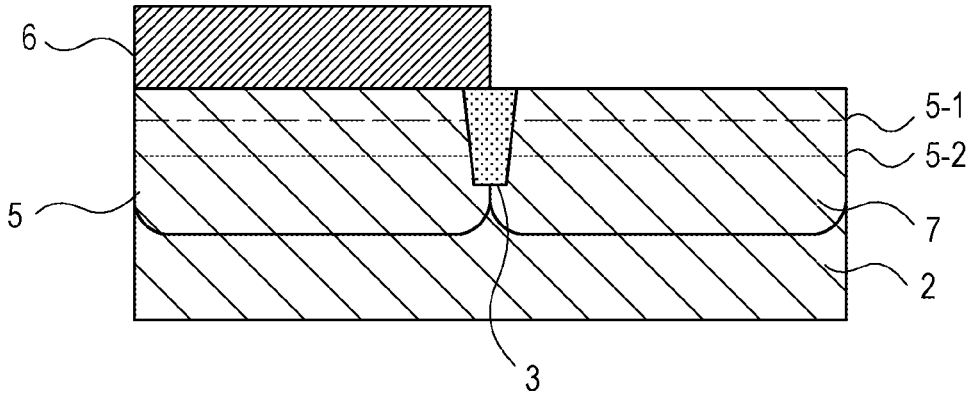


FIG. 1D

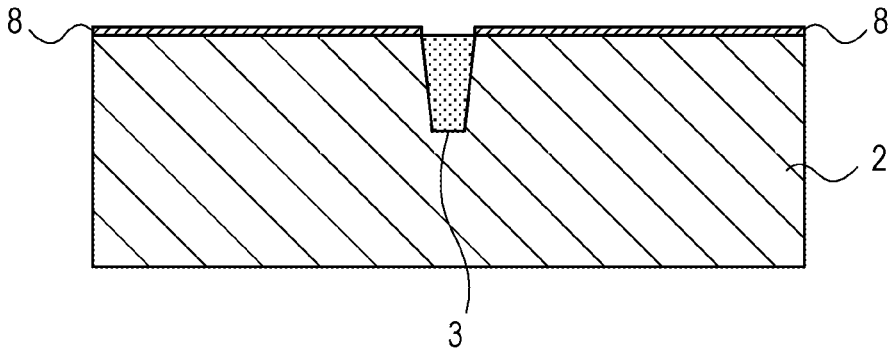


FIG. 1E

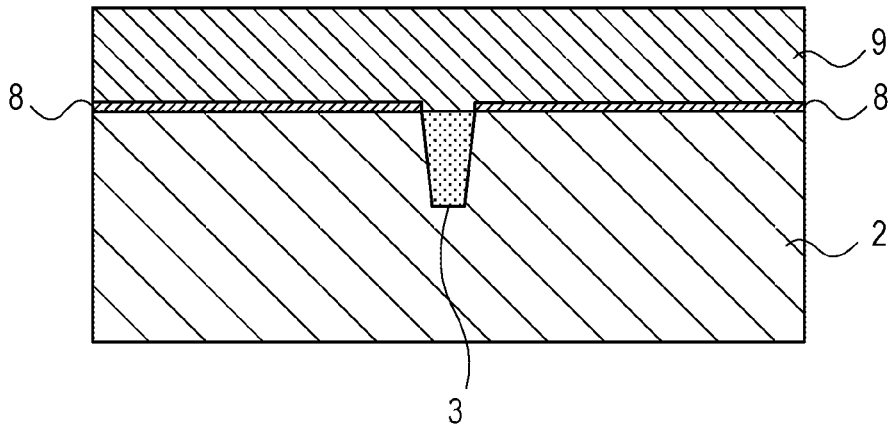


FIG. 1F

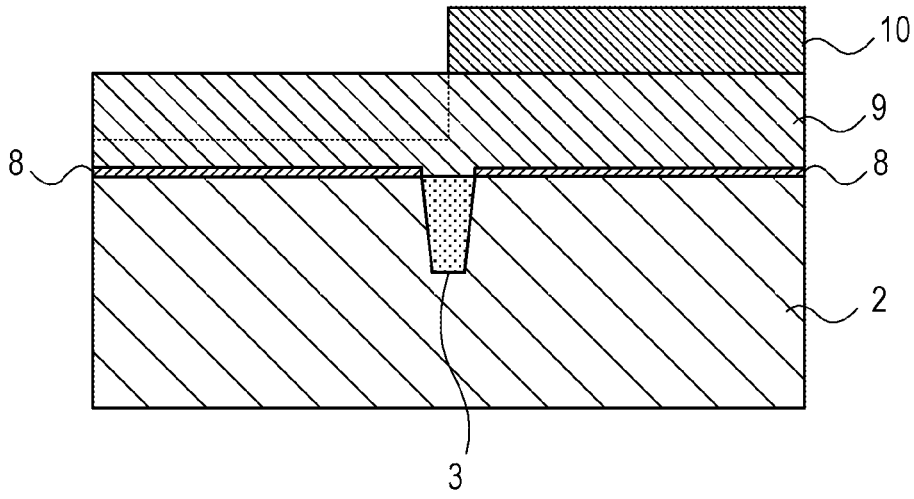


FIG. 1G

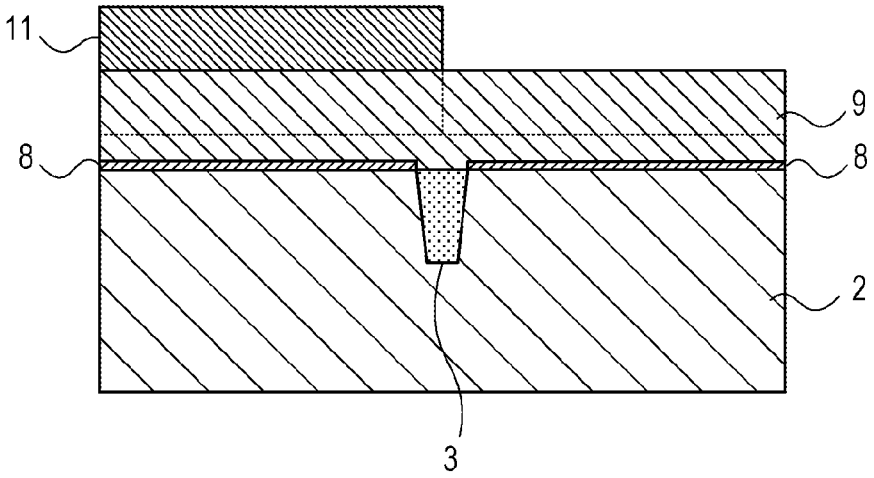


FIG. 1H

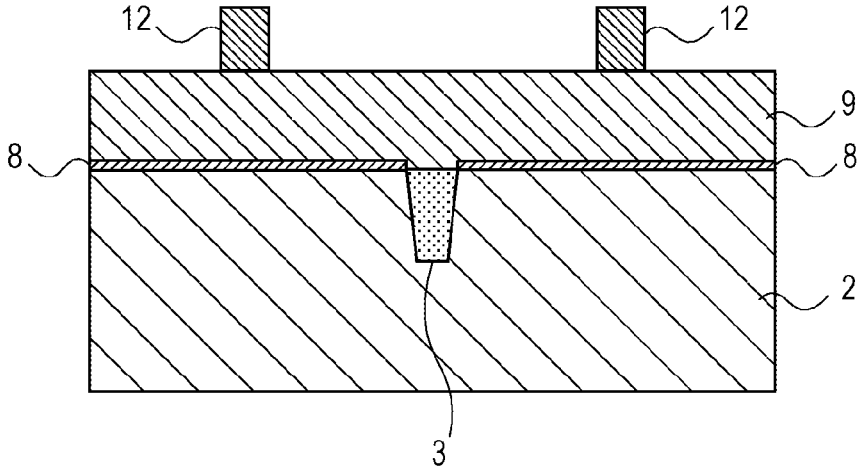


FIG. 1I

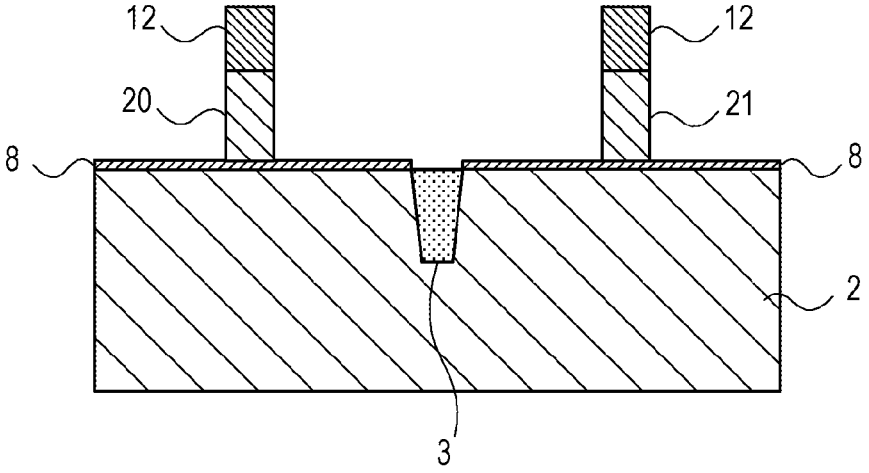


FIG. 1J

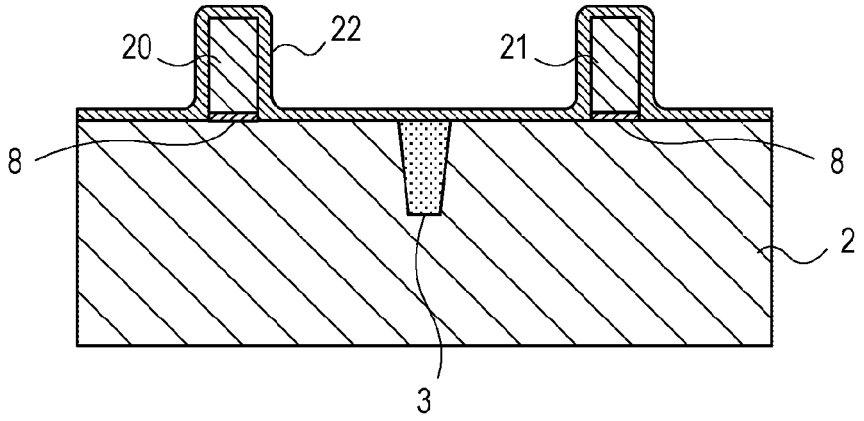


FIG. 1K

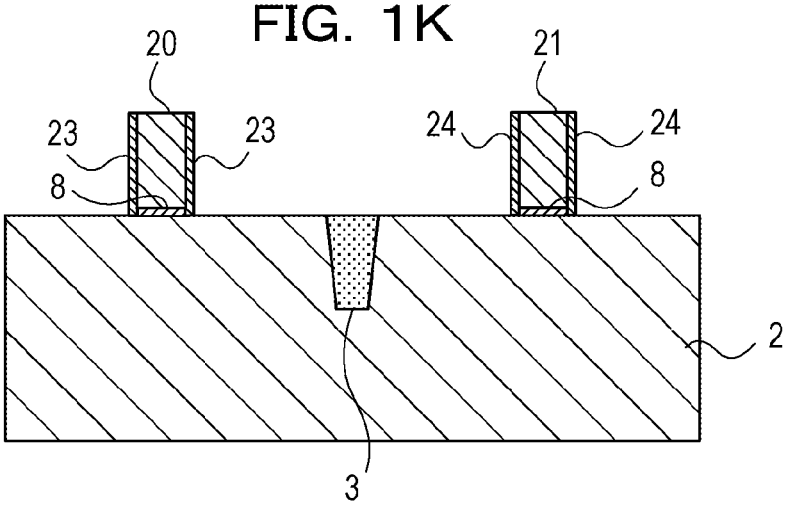


FIG. 1L

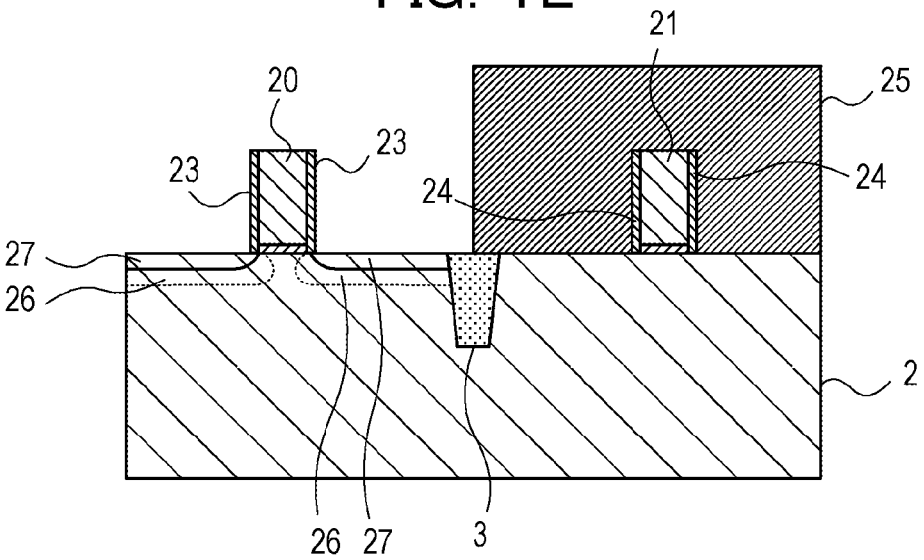


FIG. 1M

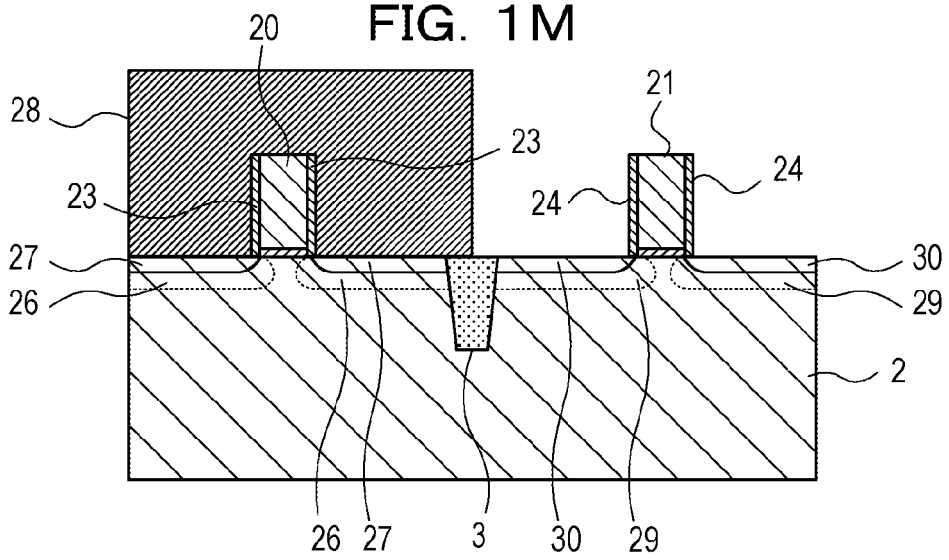


FIG. 1N

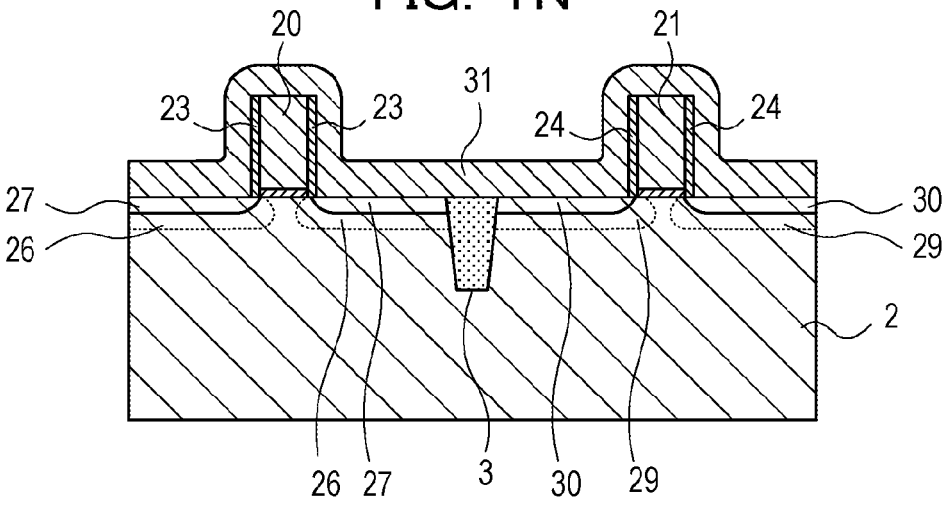


FIG. 1O

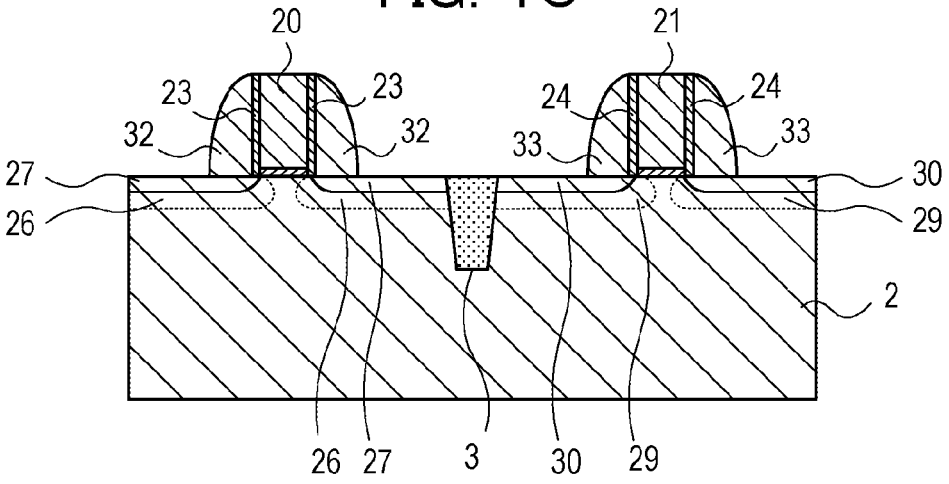


FIG. 1P

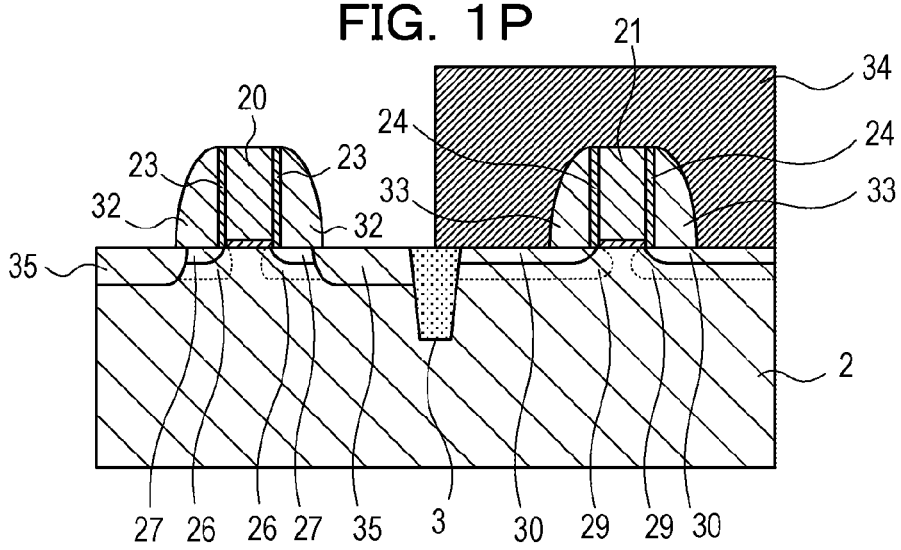
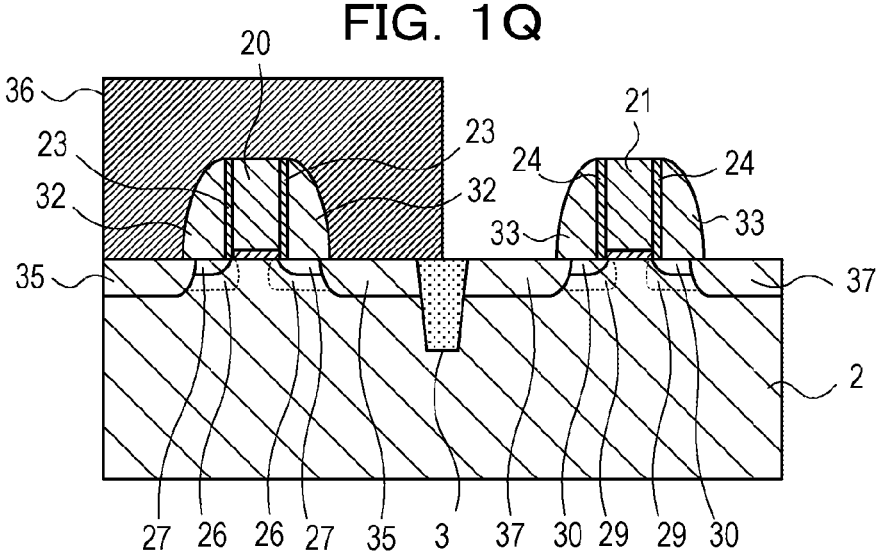


FIG. 1Q



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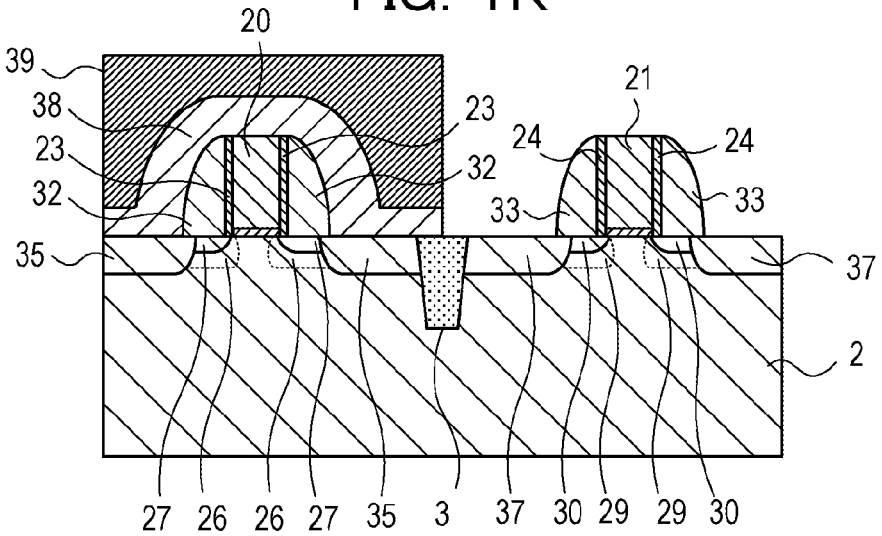


FIG. 1S

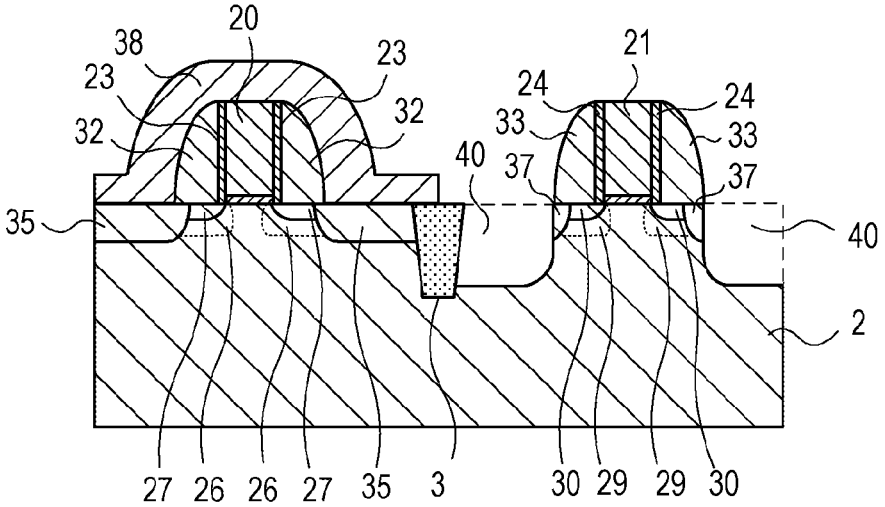


FIG. 1T

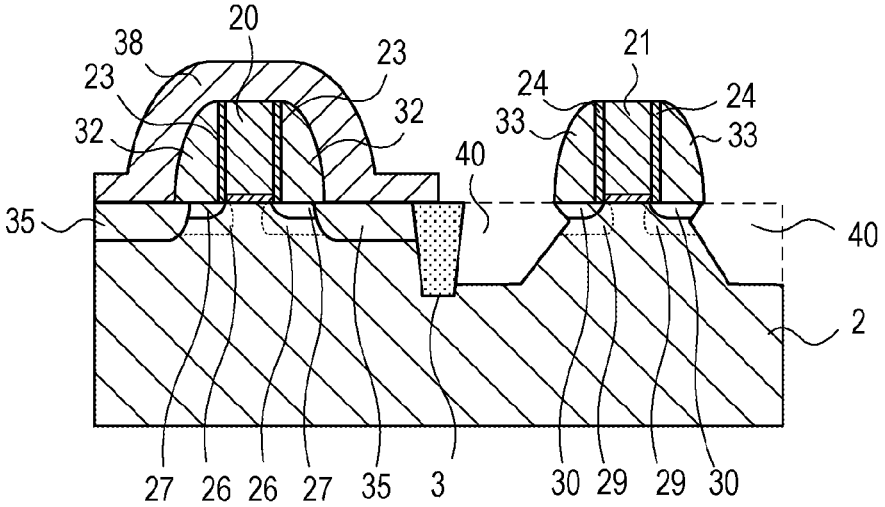


FIG. 1U

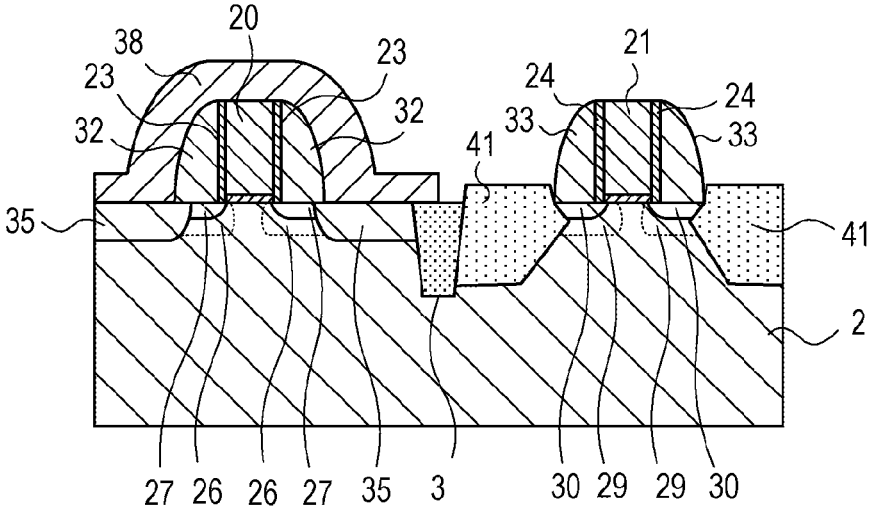
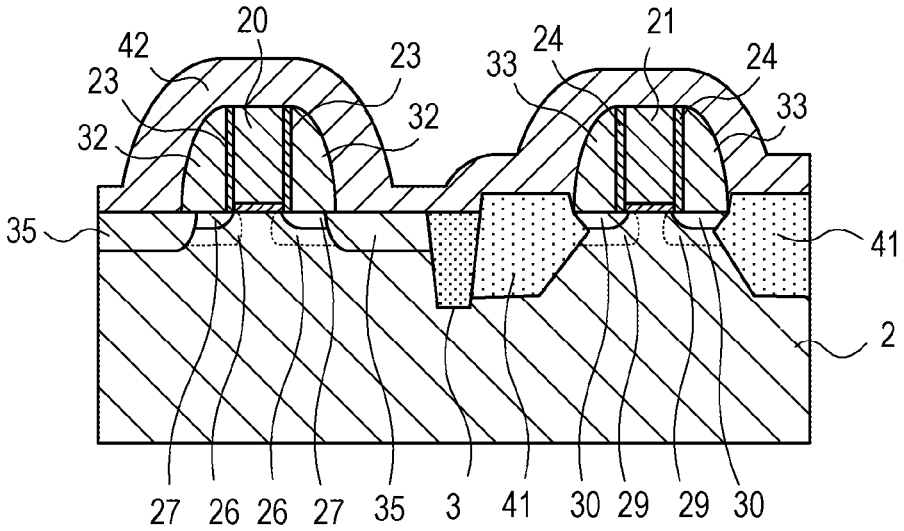


FIG. 1V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42
23
23
32
32
24
21
33
24
33
35
41
2
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26
26
27
35
3
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30
29
29
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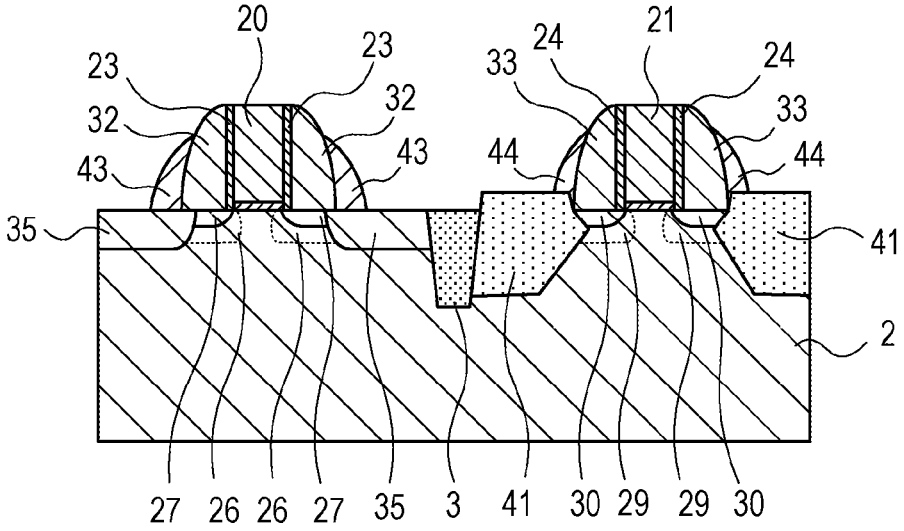
FIG. 1W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32
43
43
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21
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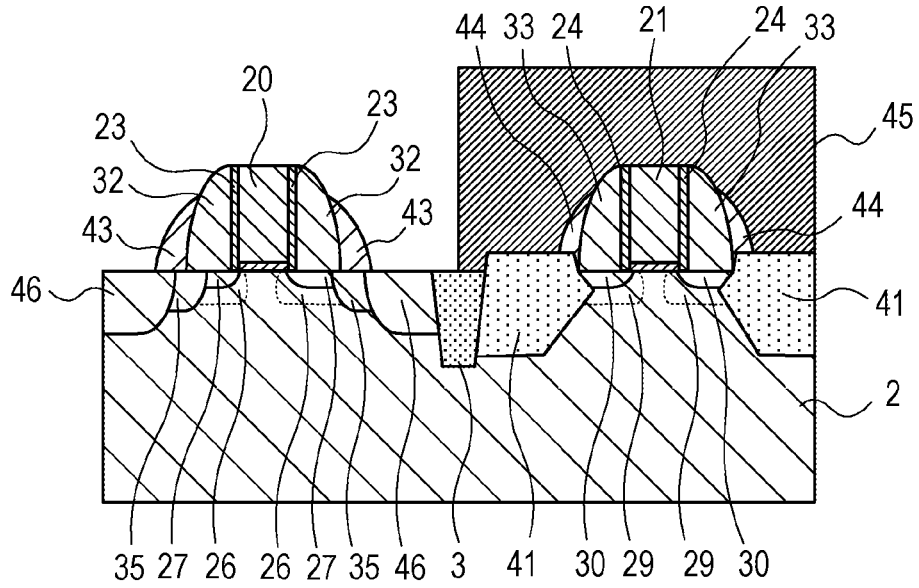
FIG. 1X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20
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23
45
32
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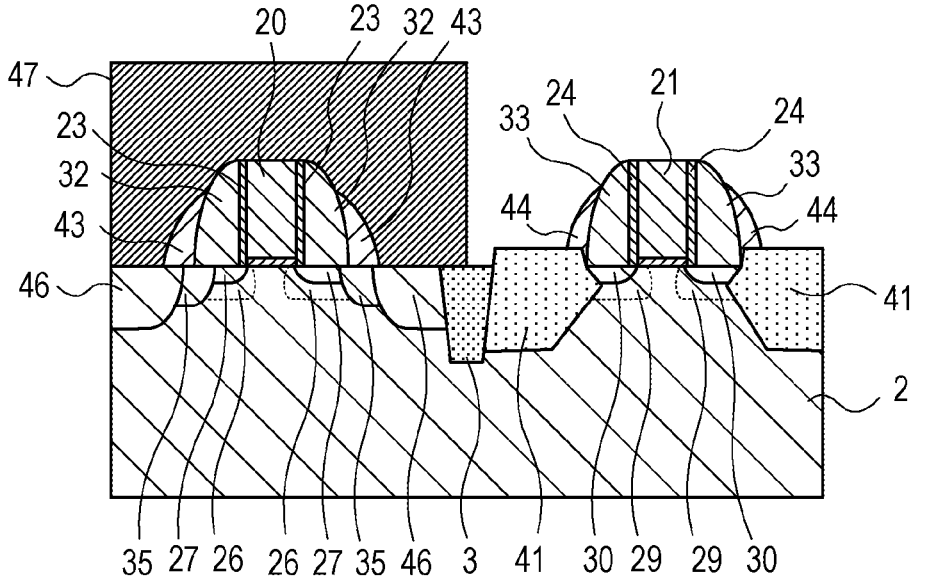
44
43
46
41
2
35 27 26 26 27 35 46 3 41 30 29 29 30

FIG. 1Y


20 23 32 43
47
24 21
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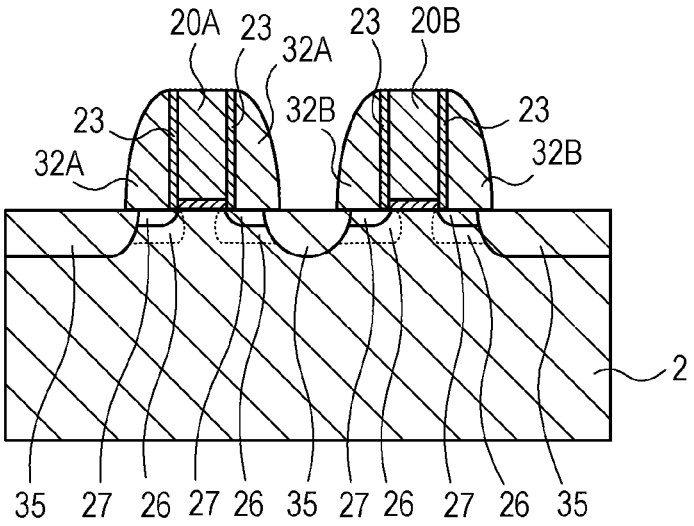
35 27 26 26 27 35 46 3 41 30 29 29 30

FIG. 2A


20A
23
32A
23
20B
23
32B
23
32A
32B
2
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27
26
27
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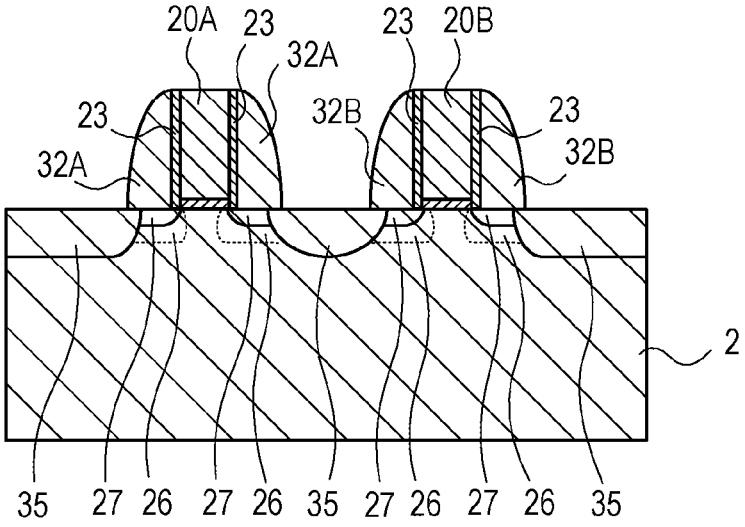
35
27
26
27
26
35

FIG. 2B


20A
23
32A
23
20B
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2
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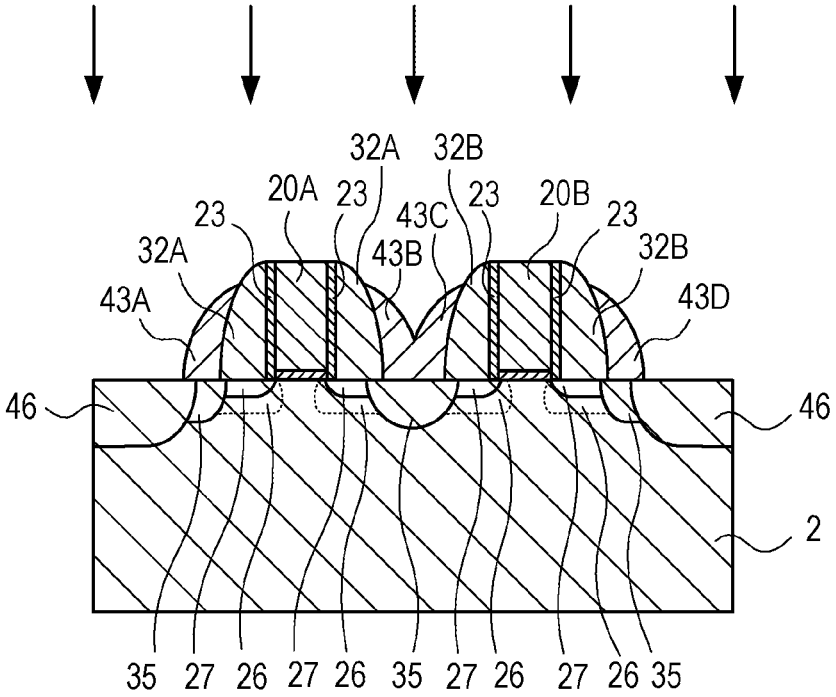
27
26
35

FIG. 2C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32B
20A
23
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43D
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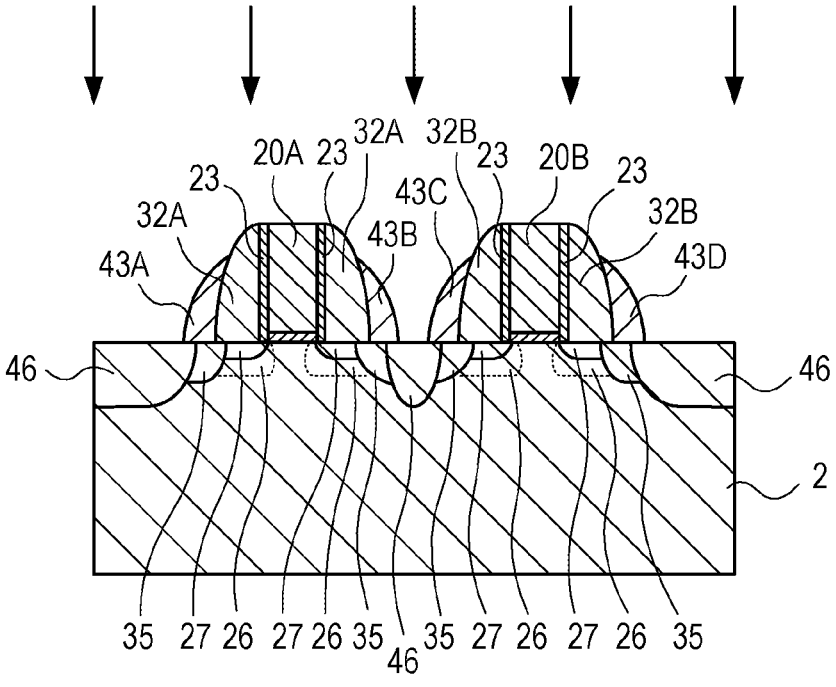
35 27 26 27 26 35 27 26 27 26 35

FIG. 2D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46
46
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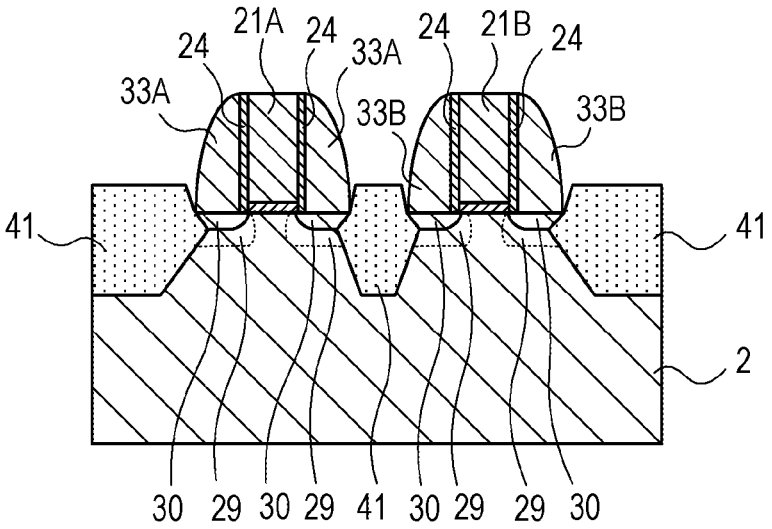
FIG. 3A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21A
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33A
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30
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29
30

FIG. 3B

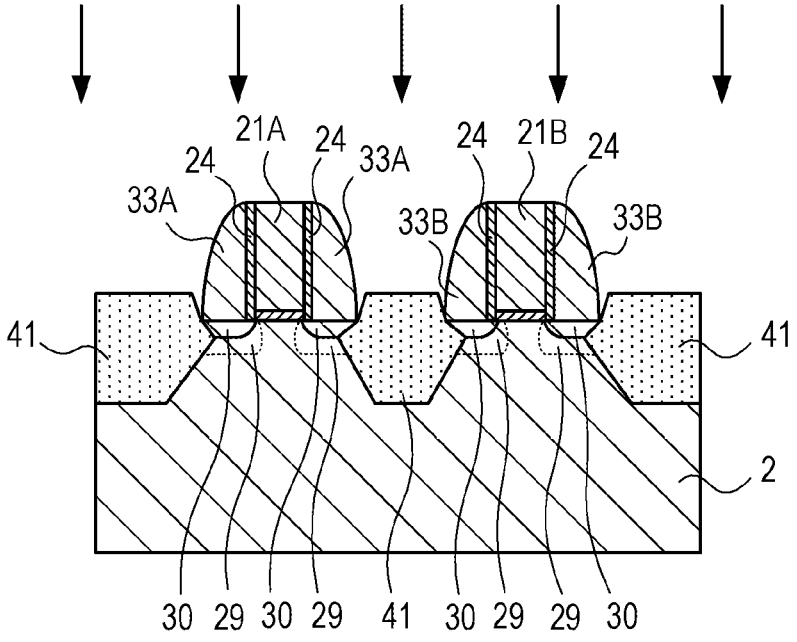
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FIG. 3C

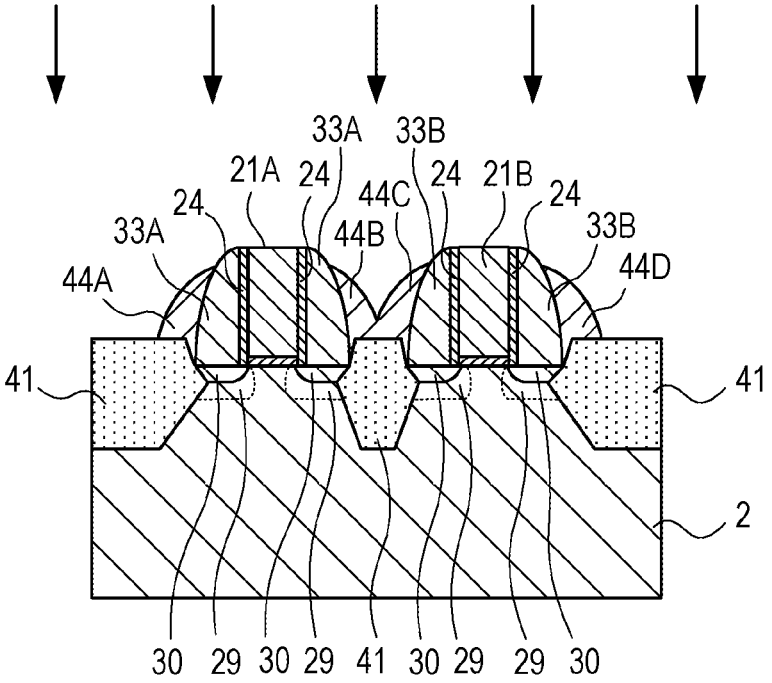
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FIG. 3D

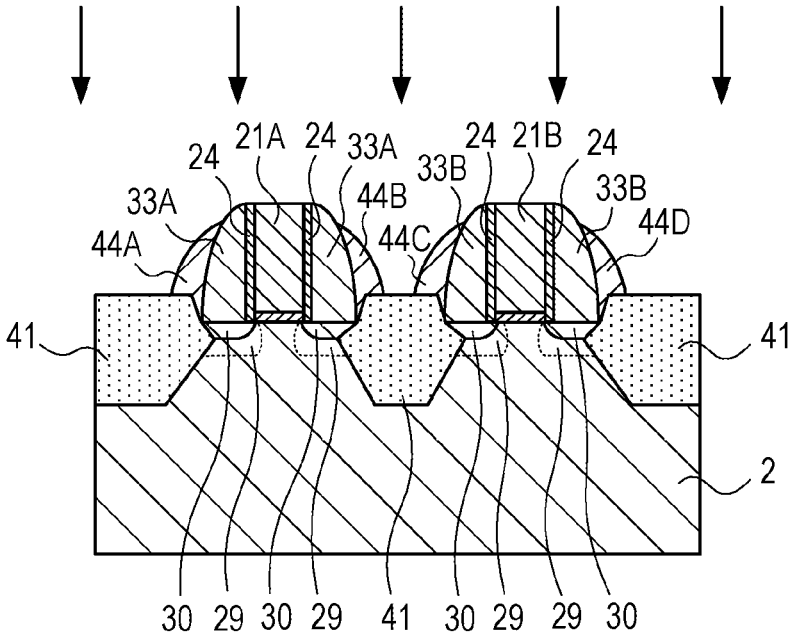
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FIG. 4A

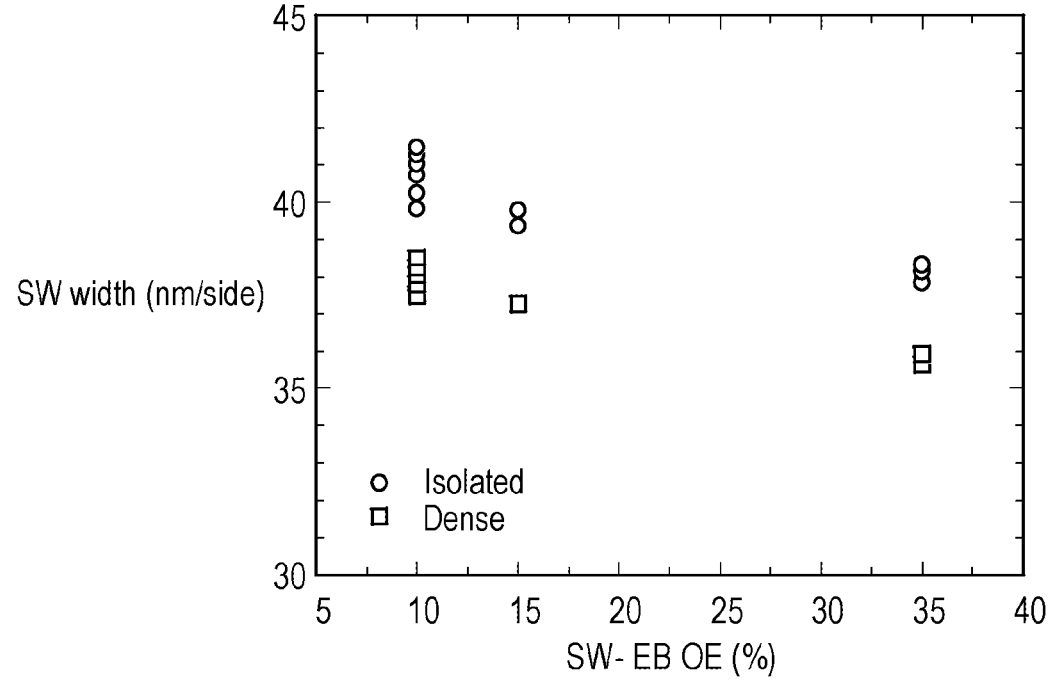

45
40
35
30
SW width (nm/side)
Isolated
Dense
5
10
15
20
25
30
35
40
SW- EB OE (%)

FIG. 4B

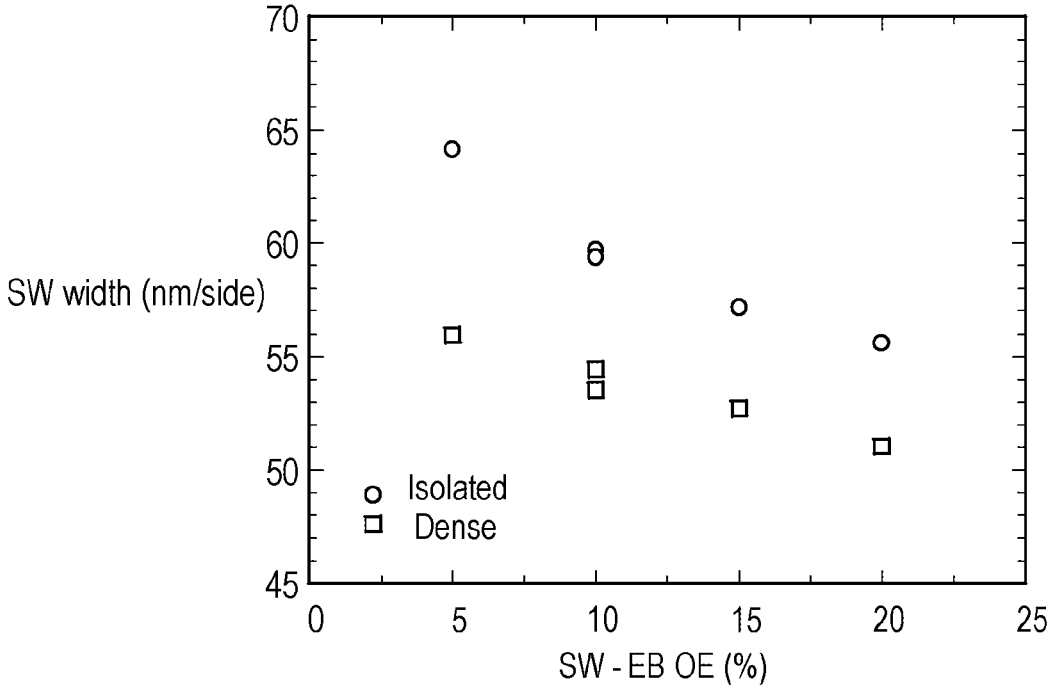

70
65
60
55
50
45
SW width (nm/side)
Isolated
Dense
0
5
10
15
20
25
SW - EB OE (%)

FIG. 5A

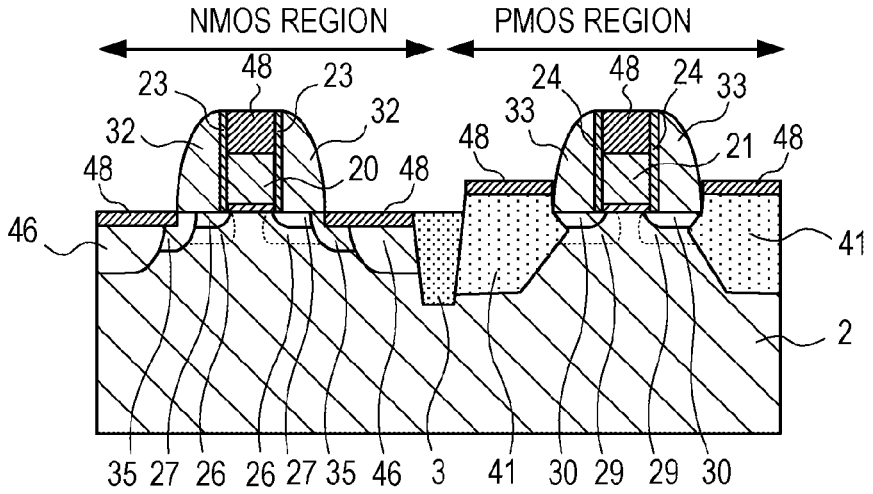


FIG. 5B

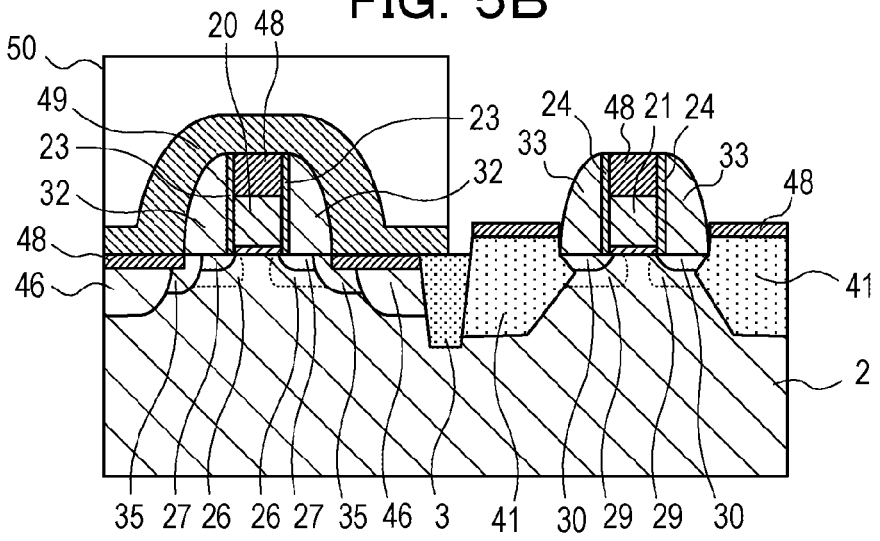


FIG. 5C

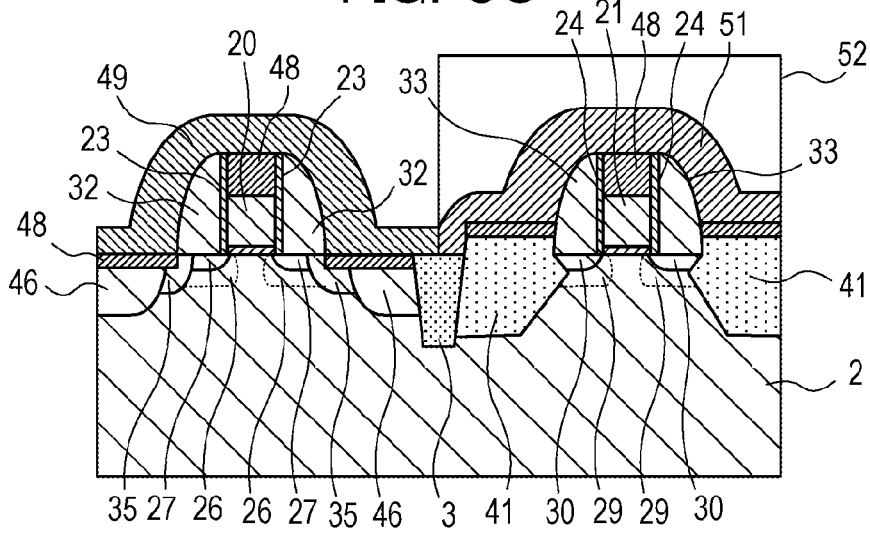


FIG. 5D

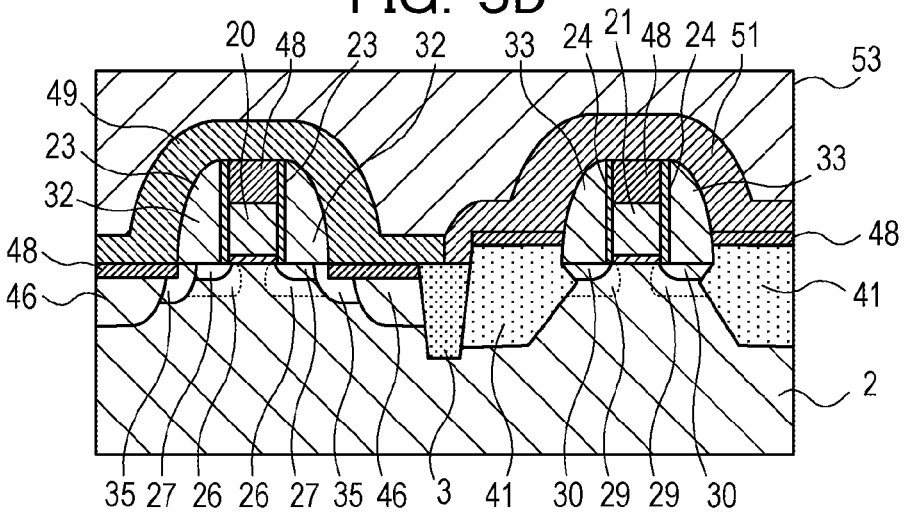


FIG. 5E

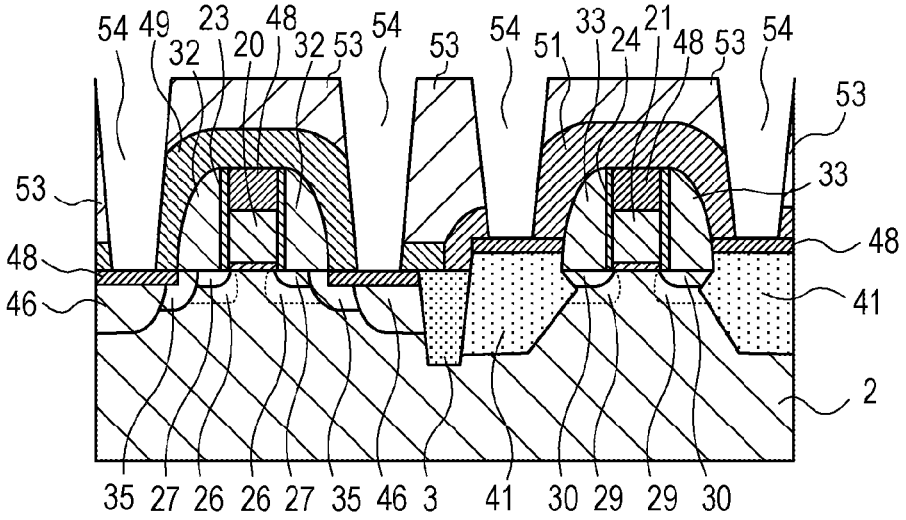


FIG. 5F

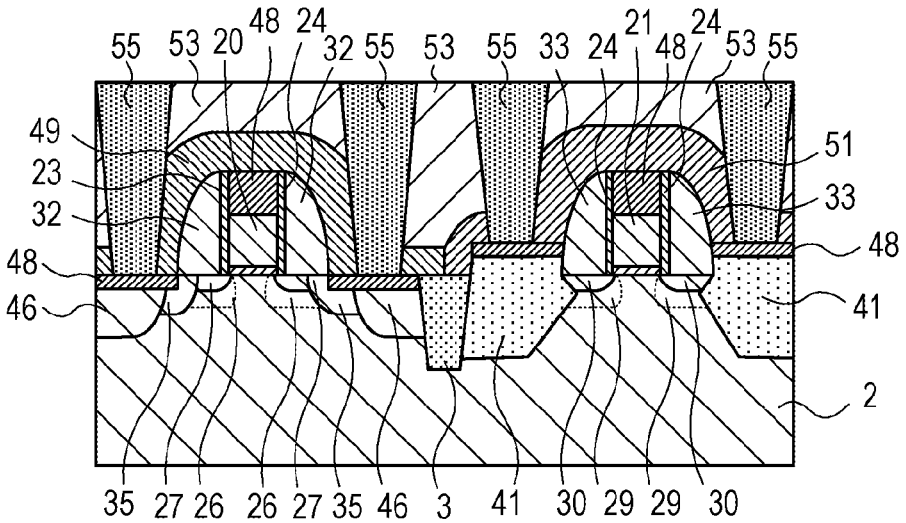


FIG. 5G

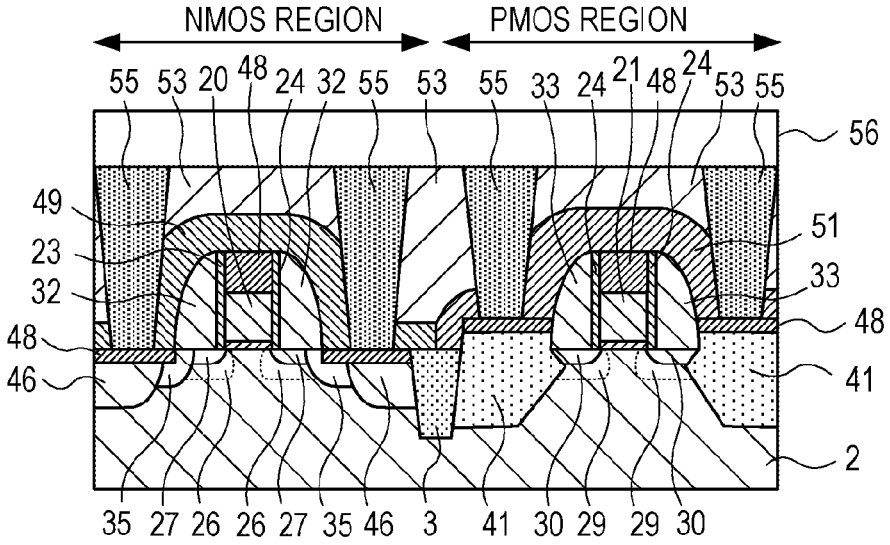


FIG. 5H

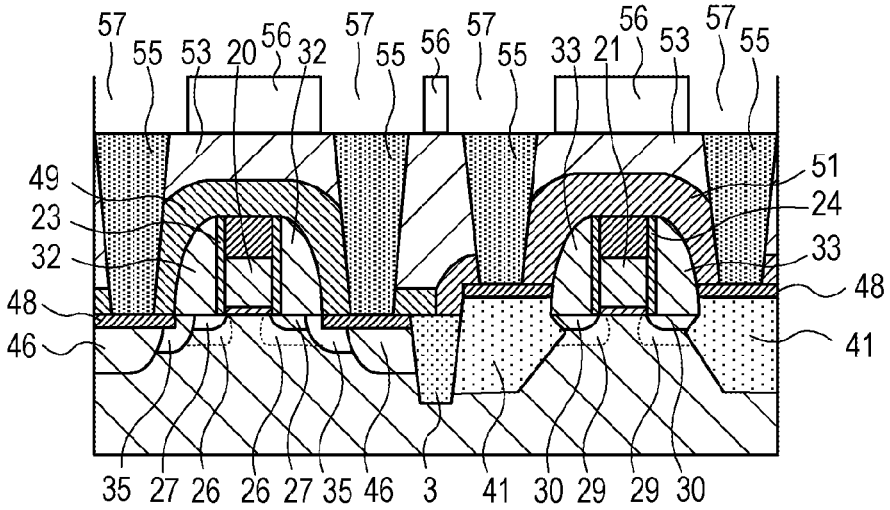
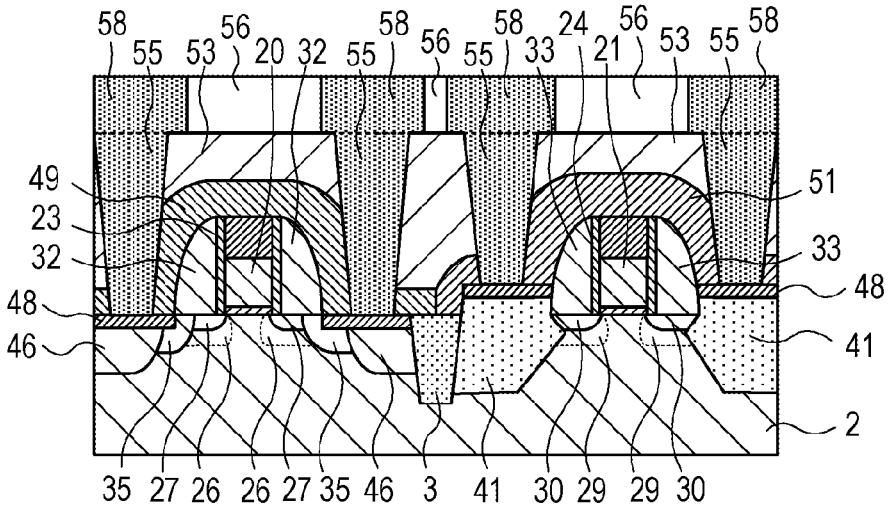


FIG. 5I



METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE INCLUDING TRENCH EMBEDDED WITH SEMICONDUCTOR LAYER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a divisional of U.S. application Ser. No. 12/544,810 (U.S. Pat. No. 8,741,711) filed Aug. 20, 2009, which is based upon and claims the benefit of priority from the prior Japanese Patent Application No. 2008-243309, filed on Sep. 22, 2008, the entire content of which is incorporated herein by reference.

FIELD

The present invention relate to a method of manufacturing a semiconductor device.

BACKGROUND

The development of the Complementary Metal-Oxide Semiconductor (CMOS) device technology has been supporting the electronics industry and engineers are adopting finer CMOS design rules at an unprecedented pace in order to further improve the performance. As for generations of CMOS devices, which are expressed in terms of technology node, volume production of the 45-nm node has been started, the 32-nm node technology has been developed, and development of the next generation or the 22-nm node has begun. The feature sizes of devices become smaller and smaller and the gate lengths of MOS transistors are now 35 nm or less.

As the feature size of devices becomes smaller, processes such as the photolithography and etching processes are becoming more difficult to perform. Source-drain impurity profiles are designed so that devices operate even when gate pitches are reduced. Sidewalls are used primarily to set an offset for regions such as source-drain regions to gate electrodes. It is known that a problem of variations in threshold voltage arises as the gate length of a MOS gate transistor decreases. The phenomenon is called the short-channel effect.

SUMMARY

According to an aspect of the invention, a method of manufacturing a semiconductor device includes forming a first and a second gate patterns, forming first and second sidewall spacers on sidewalls of the first and second gate patterns respectively, implanting a first impurity into the semiconductor substrate, forming a third sidewall spacer on the first sidewall spacer and a fourth sidewall spacer on the second sidewall spacer in such a manner that the third sidewall spacer is in contact with the fourth sidewall spacer between the first and second gate patterns, implanting a second impurity into the semiconductor substrate, and removing the third and the fourth sidewall spacers.

The object and advantages of the invention will be realized and attained by means of the elements and combinations particularly pointed out in the claims.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF DRAWINGS

FIGS. **1**A to **1**Y are cross-sectional views illustrating a process for fabricating a semiconductor device according to an embodiment;

FIGS. **2**A to **2**D are cross-sectional views illustrating a process for fabricating a semiconductor device according to an embodiment in which NMOS regions are adjacent to each other;

FIGS. **3**A to **3**D are cross-sectional views illustrating a process for fabricating a semiconductor device according to an embodiment in which NMOS regions are adjacent to each other;

FIGS. **4**A and **4**B are graphs illustrating the relationship between the overetching rate (%) of insulating film etching and the resulting sidewall spacer width; and

FIGS. **5**A to **5**I are cross-sectional views illustrating a process for fabricating a semiconductor device according to an embodiment.

DESCRIPTION OF EMBODIMENTS

Referring to FIGS. **1**A to **1**Y, a semiconductor device fabrication method according to an embodiment will be described. In the semiconductor device fabrication method according to the present embodiment, an element isolation film **3** having a Shallow Trench Isolation (STI) structure is formed in a semiconductor substrate **2** as illustrated in FIG. **1**A. For example, a resist pattern is formed over the semiconductor substrate **2** by photolithography and an element isolation trench is formed in the semiconductor substrate **2** by Reactive Ion Etching (RIE). The element isolation trench formed in the semiconductor substrate **2** is filled with silicon oxide film and a silicon oxide film is deposited over the semiconductor substrate **2** by a method such as Plasma Enhanced Chemical Vapor Deposition (PECVD).

The silicon oxide film over the semiconductor substrate **2** is planarized by Chemical Mechanical Polishing (CMP) to form an element isolation film **3** in the semiconductor substrate **2**. The formation of the element isolation film **3** in the semiconductor substrate **2** defines a region where N-type MOS transistor is to be formed (hereinafter referred to as the NMOS region) and a region where a P-type MOS transistor is to be formed (hereinafter referred to as the PMOS region) in the semiconductor substrate **2**.

Multiple NMOS and PMOS regions may be defined in the semiconductor substrate **2**. In the present embodiment, an example will be described in which NMOS and PMOS regions adjacent to each other are defined in a semiconductor substrate **2**. NMOS regions adjacent to each other may be defined in a semiconductor substrate **2**. Also, PMOS regions adjacent to each other may be defined in a semiconductor substrate **2**.

The embodiment will be described below in which NMOS transistors adjacent to each other are formed in a single active region of a semiconductor substrate **2**.

A photoresist **4** is formed over a PMOS region of a semiconductor substrate **2** by photolithography as illustrated in FIG. **1**B. The photoresist **4** is used as a mask to implant B (boron) ions with an acceleration energy of 100 keV and a dose in the range from 1×10^{13} cm^{-2} to 5×10^{13} cm^{-2} to form a P-well **5** in the NMOS region of the semiconductor substrate **2**. Channel implantation is performed in the NMOS region of the semiconductor substrate **2** to form a channel region **5**-**1**. B (boron), for example, is implanted into the NMOS region of the semiconductor substrate **2** by channel stop implantation with an acceleration energy in the range from 15 keV to 25

keV and a dose of 5×10^{12} cm^{-2} to form a channel stop region **5-2**. In order to adjust the threshold value of the NMOS transistor, B (boron) ions, for example, are implanted into the NMOS region of the semiconductor substrate **2** with an acceleration energy of 10 keV and a dose in the range from 0.5×10^{13} cm^{-2} to 2×10^{13} cm^{-2}.

Ashing or a wet process using an agent such as sulfuric acid hydrogen peroxidemixture (SPM) is performed to remove the photoresist **4** formed over the PMOS region of the semiconductor substrate **2**. A photoresist **6** is formed over the NMOS region of the semiconductor substrate **2** by photolithography as illustrated in FIG. **1**C. The photoresist **6** is used as a mask to implant P (phosphorus) ions into the PMOS region of the semiconductor substrate **2** with an acceleration energy in the range from 250 keV to 350 keV and a dose in the range from 1×10^{13} cm^{-2} to 5×10^{13} cm^{-2} to form an N-well **7** in the semiconductor substrate **2**. As (arsenic), for example, is implanted into the PMOS region **2** of the semiconductor substrate **2** by channel stop implantation with an acceleration energy in the range from 100 keV to 150 keV to form a channel stop region **5-2** and a dose in the range from 1×10^{12} cm^{-2} to 5×10^{12} cm^{-2}. In order to adjust the threshold value of the PMOS transistor, As (arsenic) ions, for example, are implanted into the PMOS region of the semiconductor substrate **2** with an acceleration energy in the range from 50 keV to 100 keV and a dose in the range from 0.5×10^{13} cm^{-2} to 2×10^{13} cm^{-2} to form a channel region **5-1**.

Ashing or a wet process using an agent such as SPM is performed to remove the photoresist **6** formed over the NMOS region of the semiconductor substrate **2**. In order to activate impurities such as B (boron), P (phosphorus), and As (arsenic) implanted in the semiconductor substrate **2**, annealing is applied to the semiconductor substrate **2** at a heat treatment temperature of 1000° C. for a treatment time of 10 seconds, for example.

A gate insulating film **8** is formed over the semiconductor substrate **2** as shown in FIG. **1**D. For example, dry oxidization is performed at approximately 900° C. to form a foundation oxide film with a thickness of approximately 1 nm over the semiconductor substrate **2**. Then, plasma nitridation is performed in an atmosphere of NO to form an oxinitride film, which is a gate insulating film **8**, on the semiconductor substrate **2**. The plasma nitridation may be performed in an atmosphere of N_2O or NH_3, instead of an atmosphere of NO. The gate oxide film **8** is not limited to an oxinitride film; the gate oxide film **8** may be a high-dielectric-constant (High-k) insulating film. The P-well **5** and the N-well **7** are not illustrated in FIG. **1**D and the subsequent figures.

A gate polysilicon **9** is deposited over the gate oxide film **8** to a thickness of approximately 100 nm by a method such as Low Pressure Chemical Vapor Deposition (LPCVD) at 600° C., for example, as illustrated in FIG. **1**E. A photoresist **10** is formed over the gate polysilicon **9** in the PMOS region by photolithography as illustrated in FIG. **1**F. The photoresist **10** is used as a mask to implant n-type impurity ions into the gate polysilicon **9** in the NMOS region. For example, As (arsenic) ions may be implanted into the gate polysilicon **9** in the NMOS region with an acceleration energy in the range from 20 keV to 30 keV and a dose in the range from 3×10^{15} cm^{-2} to 5×10^{15} cm^{-2}.

The photoresist **10** is removed by ashing or a wet process using an agent such as SPM. A photoresist **11** is formed over the gate polysilicon **9** in the NMOS region by photolithography as illustrated in FIG. **1**G. The photoresist **11** is used as a mask to implant p-type impurity ions into the gate polysilicon **9** in the PMOS region. For example, B (boron) ions may be implanted into the gate polysilicon **9** in the PMOS region with an acceleration energy in the range from 3 keV to 5 keV and a dose of 3×10^{15} cm^{-2} to 5×10^{15} cm^{-2}.

The photoresist **11** is removed by ashing or a wet process using an agent such as SPM. In order to accelerate diffusion of the n-type and p-type impurities implanted in the gate polysilicon **9** as required, spike annealing may be applied to the semiconductor substrate **2** at a heat treatment temperature of 1000° C. for a treatment time of approximately 5 seconds, for example.

As illustrated in FIG. **1**H, a photoresist **12** is formed over the gate polysilicon **9** by photolithography. An anti-reflection coating may be formed over the gate polysilicon **9** as required. If an anti-reflection coating is formed over the gate polysilicon **9**, the photoresist **12** is formed over the anti-reflection coating.

The photoresist **12** is used as a mask to anisotropically etch the gate polysilicon **9** by RIE to form gate patterns **20** and **21** as illustrated in FIG. **1**I. The gate patterns **20** and **21** are formed adjacent to each other as illustrated in FIG. **1**I. The photoresist **12** formed over the gate patterns **20** and **21** are removed by ashing or a wet process using an agent such as SPM.

As illustrated in FIG. **1**J, an insulating film **22** is formed over the entire NMOS and PMOS regions of the semiconductor substrate **2**. For example, a SiO_2 film is deposited by LPCVD, for example, from Tetra Ethyl Ortho Silicate (TEOS) over the semiconductor substrate **2** to a thickness of 10 nm, for example, at 600° C., for example. For example, a SiN film may be deposited over the semiconductor substrate **2** from dichlorsilane (SiH_2Cl_2) to a thickness of 10 nm by LPCVD at 650° C., for example.

Overall anisotropic etch back is applied to the insulating film **22** by RIE to form sidewall spacers **23** and **24** as illustrated in FIG. **1**K. That is, the sidewall film **22** is left on the sidewalls of the gate pattern **20** to form a sidewall spacer **23** and the sidewall film **22** is left on the sidewalls of the gate pattern **21** to form a sidewall spacer **24**. The sidewall film **22** and the sidewall spacers **23** and **24** are not essential to the present embodiment.

A photoresist **25** is formed over the PMOS region of the semiconductor substrate **2** by photolithography. As illustrated in FIG. **1**L, the gate pattern **20**, the sidewall spacer **23**, and the photoresist **25** are used as a mask to apply pocket implantation and extension implantation to the NMOS region of the semiconductor substrate **2**. Here, co-implantation of N (nitrogen) or Ge (germanium) may be used. In this way, the sidewall spacer **23** functions as an offset film for the pocket implantation and extension implantation in the NMOS region of the semiconductor substrate **2**. If the step of forming the sidewall spacer **23** has been omitted, the gate pattern **20** and the photoresist **25** are used as a mask to apply the pocket implantation and extension implantation to the NMOS region of the semiconductor substrate **2**.

The pocket implantation into the NMOS region of the semiconductor substrate **2** is accomplished by implanting a pocket impurity into the NMOS region of the semiconductor substrate **2**. The pocket impurity to be implanted into the NMOS region of the semiconductor substrate **2** is a p-type impurity such as B (boron) or In (indium). For example, B (boron) ions may be implanted into the NMOS region of the semiconductor substrate **2** with an acceleration energy in the range from 3 keV to 6 keV at a tilt angle in the range from 20 degrees to 30 degrees, with a doze in the range from 0.4×10^{13} cm^{-2} to 1×10^{13} cm^{-2} in four directions.

The extension implantation into the NMOS region of the semiconductor substrate **2** is accomplished by implanting an extension impurity into the NMOS region of the semiconduc-

tor substrate **2**. The extension impurity to be implanted into the NMOS region of the semiconductor substrate **2** is an n-type impurity such as P (phosphorus) or As (arsenic). For example, As (arsenic) ions may be implanted into the NMOS region of the semiconductor substrate **2** with an acceleration energy in the range from 1 kev to 3 kev and a dose in the range from $1.0'10^{15}$ cm^{-2} to 2×10^{15} cm^{-2}, for example.

The pocket impurity implantation into the NMOS region of the semiconductor substrate **2** forms a pocket region **26** in the NMOS region of the semiconductor substrate **2** as illustrated in FIG. **1**L. The extension impurity implantation into the NMOS region of the semiconductor substrate **2** forms an extension region **27** in the NMOS region of the semiconductor substrate **2** as illustrated in FIG. **1**L. The pocket impurity is implanted deeper than the extension impurity implanted in the NMOS region of the semiconductor substrate **2**.

Ashing or a wet process using an agent such as SPM is performed to remove the photoresist **25** formed over the PMOS region of the semiconductor substrate **2**. Pocket implantation and extension implantation into different NMOS regions of the semiconductor substrate **2** may be performed under different conditions. In that case, the steps of forming the photoresist **25**, performing pocket implantation into an NMOS region of the semiconductor substrate **2**, performing extension implantation into the NMOS region of the semiconductor substrate **2**, and removing the photoresist **25** are repeated as many times as required.

A photoresist **28** is formed over the NMOS region of the semiconductor substrate **2** by photolithography. As illustrated in FIG. **1**M, the gate pattern **21**, sidewall spacer **24**, and the photoresist **28** are used as a mask to apply pocket implantation and extension implantation to the PMOS region of the semiconductor substrate **2**. Here, co-implantation of a material such as C (carbon) or Ge (germanium) may be used. In this way, the sidewall spacer **24** functions as an offset for performing pocket implantation and extension implantation into the PMOS region of the semiconductor substrate **2**. If the step of forming the sidewall spacer **24** has been omitted, the gate pattern **21** and the photoresist **28** are used as a mask to perform the pocket implantation and extension implantation into the PMOS region of the semiconductor substrate **2**.

The pocket implantation into the PMOS region of the semiconductor substrate **2** is accomplished by implanting a pocket impurity into the PMOS region of the semiconductor substrate **2**. The pocket impurity to be implanted into the PMOS region of the semiconductor substrate **2** is an n-type impurity such as (arsenic) or Sb (antimony). For example, As (arsenic) ions may be implanted into the PMOS region of the semiconductor substrate **2** with an acceleration energy in the range from 25 keV to 40 keV at a tilt angle in the range from 20 degrees to 30 degrees with a dose in the range from 0.4×10^{13} cm^{-2} to 1×10^{13} cm^{-2} in four directions.

The extension implantation into the PMOS region of the semiconductor substrate **2** is accomplished by implanting an extension impurity into the PMOS region of the semiconductor substrate **2**. The extension impurity to be implanted into the PMOS region of the semiconductor substrate **2** is a p-type impurity such as boron (B). For example, B (boron) ions may be implanted into the PMOS region of the semiconductor substrate **2** with an acceleration energy of 0.5 keV with a dose in the range from 1.0×10^{15} cm^{-2} to 2×10^{15} cm^{-2}.

The implantation of pocket impurity into the PMOS region of the semiconductor substrate **2** forms a pocket region **29** in the PMOS region of the semiconductor substrate **2** as illustrated in FIG. **1**M. The implantation of extension impurity into the PMOS region of the semiconductor substrate **2** forms an extension region **30** in the PMOS region of the semiconductor substrate **2** as illustrated in FIG. **1**M. The pocket impurity ions are implanted into the PMOS region of the semiconductor substrate **2** deeper than the extension impurity implanted in the PMOS region of the semiconductor substrate **2**.

Ashing or a wet process using an agent such as SPM is performed to remove the photoresist **28** formed over the NMOS region of the semiconductor substrate **2**. Pocket implantation and extension implantation into different PMOS regions of the semiconductor substrate **2** may be performed under different conditions. In this case, the steps of forming photoresist **28**, performing pocket implantation into the PMOS regions of the semiconductor substrate **2**, performing extension implantation into the PMOS regions of the semiconductor substrate **2**, and removing the photoresist **28** are repeated as many times as required.

An insulating film **31** is formed to cover the semiconductor substrate **2**, the gate patterns **20**, **21**, and the sidewall spacers **23**, **24** as illustrated in FIG. **1**N. That is, the sidewall film **31** is formed over the entire NMOS and PMOS regions of the semiconductor substrate **2**. For example, a SiON film may be deposited over the semiconductor substrate **2** to a thickness in the range from 20 nm to 40 nm by LPCVD at a low temperature of less than or equal to approximately 600° C. to form the insulating film **31**. If the step of forming the sidewall spacers **23** and **24** has been omitted, the insulating film **31** is formed to cover the semiconductor substrate **2** and the gate patterns **20** and **21**. The insulating film **31** may be exposed to an HF solution in a subsequent process step. The insulating film **31** may be made of SiN because SiN is highly resistant to solutions such as an HF solution.

As illustrated in FIG. **10**, overall anisotropic etch back is applied to the insulating film **31** by RIE to form sidewall spacers **32** and **33**.

A photoresist **34** is formed over the PMOS region of the semiconductor substrate **2** by photolithography. As illustrated in FIG. **1**P, the gate pattern **20**, the sidewall spacers **23**, **32**, and the photoresist **34** are used as a mask to perform buffer implantation into the NMOS region of the semiconductor substrate **2**. In this way, the sidewall spacer **32** functions as an offset film for buffer implantation into the NMOS region of the semiconductor substrate **2**. If the step of forming the sidewall spacer **23** has been omitted, the gate pattern **20**, the sidewall spacer **32**, and the photoresist **34** are used as a mask to perform buffer implantation into the NMOS region of the semiconductor substrate **2**.

The buffer implantation into the NMOS region of the semiconductor substrate **2** is accomplished by implanting a buffer impurity into the NMOS region of the semiconductor substrate **2**. The buffer impurity to be implanted into the NMOS region of the semiconductor substrate **2** is an n-type impurity such as (arsenic). For example, As (arsenic) ions may be implanted into the NMOS region of the semiconductor substrate **2** with an acceleration energy of 10 keV to 15 keV and a dose in the range from 1×10^{15} cm^{-2} to 5×10^{15} cm^{-2}.

The buffer impurity implantation into the NMOS region of the semiconductor substrate **2** forms a buffer region **35** in the NMOS region of the semiconductor substrate **2** as illustrated in FIG. **1**P. The buffer impurity is implanted into the NMOS region of the semiconductor substrate **2** deeper than the extension impurity implanted in the NMOS region of the semiconductor substrate **2**.

Ashing or a wet process using an agent such as SPM is performed to remove the photoresist **34** formed over the PMOS region of the semiconductor substrate **2**. Then, a photoresist **36** is formed over the NMOS region of the semiconductor substrate **2** by photolithography. The gate pattern **21**,

the sidewall spacers **24** and **33**, and the photoresist **36** are used as a mask to perform buffer implantation into the PMOS region of the semiconductor substrate **2**. In this way, the sidewall spacer **33** functions as an offset film for buffer implantation into the PMOS region of the semiconductor substrate **2**. If the step of forming the sidewall spacer **24** has been omitted, the gate pattern **21**, sidewall spacer **33**, and the photoresist **36** are used as a mask to perform buffer implantation into the PMOS region of the semiconductor substrate **2**.

The buffer implantation into the PMOS region of the semiconductor substrate **2** is accomplished by implanting a buffer impurity into the PMOS region of the semiconductor substrate **2**. The buffer impurity to be implanted into the PMOS region of the semiconductor substrate **2** is a p-type impurity such as B (boron). For example, B (boron) ions may be implanted into the PMOS region of the semiconductor substrate **2** with an acceleration energy in the range from 10 keV to 15 keV and a dose in the range from 1×10^{15} cm^{-2} to 5×10^{15} cm^{-2}.

The buffer impurity implantation into the PMOS region of the semiconductor substrate **2** forms a buffer region **37** in the PMOS region of the semiconductor substrate **2** as illustrated in FIG. **1**Q. The buffer impurity is implanted into the PMOS region of the semiconductor substrate **2** deeper than the extension impurity implanted in the PMOS region of the semiconductor substrate **2**.

Ashing or a wet process using an agent such as SPM is performed to remove the photoresist **36** formed over the NMOS region of the semiconductor substrate **2**. A cap film **38** is formed over the entire NMOS and PMOS regions of the semiconductor substrate **2**. For example, a SiO_2 film may be deposited by LPCVD over the semiconductor substrate **2** to a thickness of 50 nm at a low temperature lower than or equal to 550° C. to form the cap film **38**. If the step of forming the sidewall spacers **23** and **24** has been omitted, the cap film **38** is formed to cover the semiconductor substrate **2**, the gate patterns **20**, **21**, and the sidewall spacers **32** and **33**.

A photoresist **39** is formed over the NMOS region of the semiconductor substrate **2** by photolithography. As illustrated in FIG. **1**R, the photoresist **39** is used as a mask to perform anisotropic etching of the cap film **38** in the PMOS region of the semiconductor substrate **2** by RIE to remove the cap film **38** from the PMOS region of the semiconductor substrate **2**. In this way, the photoresist **39** formed over the NMOS region of the semiconductor substrate **2** functions as a mask in removing the cap film **38** in the PMOS region of the semiconductor substrate **2**. The photoresist **39** may be selectively formed over multiple NMOS regions of the semiconductor substrate **2**. With this, the cap film **38** may be selectively removed from the multiple NMOS regions of the semiconductor substrate **2**.

Ashing or a wet process using an agent such as SPM is performed to remove the photoresist **39** formed over the NMOS region of the semiconductor substrate **2**. As illustrated in FIG. **1**S, the gate pattern **21**, the sidewall spacers **24** and **33**, and the cap film **38** are used as a mask to perform anisotropic etching of the PMOS region of the semiconductor substrate **2** by RIE to form a trench **40** in the PMOS region of the semiconductor substrate **2**.

As illustrated in FIG. **1**T, the trench **40** formed in the PMOS region of the semiconductor substrate **2** is horizontally extended by wet etching. That is, the trench **40** formed in the PMOS region of the semiconductor substrate **2** is processed by wet etching so that the sidewall of the trench **40** is shaped like a letter E. The trench **40** formed in the PMOS region of the semiconductor substrate **2** is shaped in this way in order to efficiently apply a strain to the channel in the PMOS region of the semiconductor substrate **2**. The shaping of the trench **40** formed in the PMOS region of the semiconductor substrate **2** may be performed as required. Therefore the step of shaping of the trench **40** formed in the PMOS region of the semiconductor substrate **2** may be omitted.

SiGe (silicon germanium) is selectively epitaxially grown in the trench **40** formed in the PMOS region of the semiconductor substrate **2**. By epitaxially growing SiGe in the trench **40** formed in the PMOS region of the semiconductor substrate **2**, a SiGe layer **41** is formed in the PMOS region of the semiconductor substrate **2** as illustrated in FIG. **1**U. During the epitaxial growth of SiGe, the PMOS region of the semiconductor substrate **2** may be in situ doped with B (boron). If the PMOS region of the semiconductor substrate **2** is in-situ doped with B (boron) in the silicon germanium layer **41** forming process, the step of performing buffer implantation into the PMOS region of the semiconductor substrate **2** may be omitted.

Because the lattice constant of $Si_{1-x}Ge_x$ (x=0.1 to 0.3) is greater than that of Si, a compressive strain is caused in the depth direction and a tensile strain is cased in the horizontal direction. As a result, the compressive strain is applied along the channel direction, which increases the hole mobility. The width of the sidewall spacer **33** is set so that a desired distance between the silicon germanium layer **41** and the channel is provided. In order to suppress the growth of SiGe on the gate pattern **21**, an insulating film of a material such as SiO_2 may be formed over the gate pattern **21** before SiGe is epitaxially grown.

By a wet process using an HF solution, the cap film **38** is removed from the PMOS region of the semiconductor substrate **2**. An insulating film **42** is formed over the entire NMOS and PMOS regions of the semiconductor substrate **2** as illustrated in FIG. **1**V. For example, a SiO_2 film may be deposited over the semiconductor substrate **2** by LPCVD at a temperature equal to or less than 550° C. to a thickness of 50 nm to form the insulating film **42**. If the step of forming the sidewall spacers **23** and **24** has been omitted, the insulating film **42** is formed to cover the semiconductor substrate **2**, gate patterns **20**, **21**, and the sidewall spacers **32**, **33**. Because the insulating film **42** is removed in a subsequent process step, the sidewall film **42** is preferably formed of SiO_2 film, which may be removed with an HF solution.

As illustrated in FIG. **1**W, overall anisotropic etch back is applied to the insulating film **42** by RIE to form sidewall spacers **43** and **44**.

A photoresist **45** is formed in the PMOS region over the semiconductor substrate **2** by photolithography. As illustrated in FIG. **1**X, the gate pattern **20**, the sidewall spacers **23**, **32**, **43**, and the photoresist **45** are used as a mask to perform deep-source-drain (SD) impurity implantation into the NMOS region of the semiconductor substrate **2**. In this way, the sidewall spacer **43** functions as an offset film in deep-SD impurity implantation into the NMOS region of the semiconductor substrate **2**. If the step of forming the sidewall spacer **23** has been omitted, the gate pattern **20**, the sidewall spacers **32** and **43**, and the photoresist **45** are used as a mask to perform the deep-SD impurity implantation into the NMOS region of the semiconductor substrate **2**. The distance between the deep-SD region **46** and the end of the gate pattern **20** may be controlled by the widths of the sidewall spacers **43**, **23** and **32**. In the present embodiment, an offset between the deep-SD region **46** and the end of the gate pattern **20** in the NMOS region may be set by the provision of the sidewall spacer **43**, independently of an offset between the silicon germanium layer **41** and a channel region in the PMOS region.

The deep-SD impurity implantation into the NMOS region of the semiconductor substrate **2** is accomplished by implanting a deep-SD impurity into the NMOS region of the semiconductor substrate **2**. The deep-SD impurity to be implanted into the NMOS region of the semiconductor substrate **2** is an n-type impurity such as P (phosphorus). For example, P (phosphorus) ions may be implanted into the NMOS region of the semiconductor substrate **2** with an acceleration energy in the range from 5 keV to 10 keV and a dose in the range from 1×10^{15} cm^{-2} to 5×10^{15} cm^{-2}.

The deep-SD impurity implantation into the NMOS region of the semiconductor substrate **2** forms the deep-SD region **46** in the NMOS region of the semiconductor substrate **2** as illustrated in FIG. **1**X. Since the deep-SD impurity is implanted into the NMOS region of the semiconductor substrate **2** deeper than the extension impurity implanted in the NMOS region of the semiconductor substrate **2**, the deep-SD region **46** extends to a depth deeper than the extension region **27**. In other words, since the extension impurity is implanted into the NMOS region of the semiconductor substrate **2** shallower than the deep-SD impurity implanted in the NMOS region of the semiconductor substrate **2**, the extension region **27** is formed to a depth shallower than the deep-SD region **46**.

Since the deep-SD impurity is implanted into the NMOS region of the semiconductor substrate **2** deeper than the buffer impurity implanted in the NMOS region of the semiconductor substrate **2**, the deep-SD region **46** extends to a depth deeper than the buffer region **35**. In other words, since the buffer impurity is implanted into the NMOS region of the semiconductor substrate **2** shallower than the deep-SD impurity implanted in the NMOS region of the semiconductor substrate **2**, the buffer region **35** is formed to a depth shallower than the deep-SD region **46**.

A photoresist **47** is formed over the NMOS region of the semiconductor substrate **2** by photolithography as illustrated in FIG. **1**Y. The gate pattern **21**, sidewall spacers **24**, **33**, and **44** and the photoresist **47** are used as a mask to implant a deep-SD impurity into the epitaxial layer **41** in the PMOS region of the semiconductor substrate **2**. For example, B (boron) ions may be implanted as the deep-SD impurity into the PMOS region of the semiconductor substrate **2**.

The sidewall spacer **44** functions as an offset film for deep-SD impurity implantation into the PMOS region of the semiconductor substrate **2**. If the step of forming the sidewall spacer **24** has been omitted, the gate pattern **21**, sidewall spacers **33** and **44**, and the photoresist **47** are used as a mask to implant the deep-SD impurity into the PMOS region of the semiconductor substrate **2**.

If the PMOS region of the semiconductor substrate **2** has been doped in situ with B (boron) in the step of forming the epitaxial layer **41**, the deep-SD impurity may not be implanted into the PMOS region of the semiconductor substrate **2** in addition. However, even if the PMOS region has been doped in situ with B (boron) in the step of forming the epitaxial layer **41**, the PMOS region of the semiconductor substrate **2** may be further implanted with the deep-SD impurity in order to reduce bonding leakage or adjust bonding capacity.

An example in which multiple NMOS regions adjacent to each other are formed and an example in which multiple PMOS regions adjacent to each other are formed will be described. FIGS. **2**A to **2**D illustrate an example in which two adjacent NMOS regions are formed in a semiconductor substrate **2**. FIGS. **3**A to **3**D illustrate an example in which two adjacent PMOS regions are formed in a semiconductor substrate **2**.

Sidewall spacers **43** and **44** are formed by forming an insulating film **42** over the entire NMOS and PMOS regions of the semiconductor substrate **2** and applying overall anisotropic etch back to the insulating film **42** as described above. In the etching step for forming the sidewall spacers **43** and **44**, the width of the insulating film remaining as the sidewall spacers depends on the gate pitch. The smaller the gate pitch is, the smaller the width of the sidewall spacer will be.

If the pitch between gate patterns **20**A and **20**B is small as illustrated in FIG. **2**A, the width of the sidewall spacer **43** formed between the gate patterns **20**A and **20**B may be small. The region between gate patterns **20**A and **20**B where the width of a sidewall spacer **43** formed between the gate patterns **20**A and **20**B will be small is herein referred to as a "narrow pitch region".

As illustrated in FIG. **2**B, if the pitch between the gate patterns **20**A and **20**B is larger than the gate pitch illustrated in FIG. **2**A, the width of the sidewall spacer **43** formed between the gate patterns **20**A and **20**B will not be small. The region between gate patterns **20**A and **20**B where the width of a sidewall spacer **43** formed between the gate patterns **20**A and **20**B is not small is herein referred to as a "wide pitch region".

In order to suppress the short-channel effect of a MOS transistor, it is important to set the width of the sidewall spacer **43** to a proper value. For example, if a deep-SD impurity is implanted into an NMOS region in a narrow pitch region of the semiconductor substrate **2** under the same conditions for deep-SD impurity implantation into an NMOS region in a wide pitch region of the semiconductor substrate **2**, the short-channel characteristics will degrade because the width of the sidewall spacer **43** in the narrow pitch region is small.

In the present embodiment, if the region between gate patterns **20**A and **20**B is a narrow pitch region as illustrated in FIG. **2**C, sidewall spacers **43**B and **43**C in the narrow pitch region are formed in such a manner that sidewall spacers **43**B and **43**C are in contact with each other. By forming the sidewall spacers **43**B and **43**C in the narrow pitch region in contact with each other, deep-SD impurity implantation into the narrow pitch region of the semiconductor substrate **2** may be reduced. As a result, degradation of the short-channel characteristics may be reduced. Although the deep-SD region **46** is not formed in a region where a narrow-pitch gate pattern **20** is formed as illustrated in FIG. **2**C, the resistance of the source-drain region may be reduced because a buffer region **35**, which is an impurity diffusion region, is formed.

Thus, an NMOS region of the semiconductor substrate **2** where a deep-SD impurity is not implanted may be used for a circuit, for example an SRAM, for which the short-channel effect has higher priority than a driving current.

If the pitch between gate patterns **20**A and **20**B is large enough as illustrated in FIG. **2**D, a deep-SD impurity may be implanted into the NMOS region of the semiconductor substrate **2** even if sidewall spacers **43**B and **43**C are formed.

If the pitch between gate patterns **21**A and **21**B is small as illustrated in FIG. **3**A, the width of the sidewall spacer **44** formed between the gate patterns **21**A and **21**B will be small.

If the pitch between gate patterns **21**A and **21**B is large enough as illustrated in FIG. **3**B, the width of the sidewall spacer **44** formed between the gate patterns **21**A and **21**B will not be small.

In order to reduce the short-channel effect, it is important to set the width of the sidewall spacer **44** to a proper value. For example, if a deep-SD impurity is implanted into a PMOS region of the semiconductor substrate **2** in a narrow pitch region under the same conditions for deep-SD impurity implantation into a PMOS region of the semiconductor sub-

strate **2** in a wide pitch region, the short-channel characteristics will degrade because the width of the sidewall spacer **44** in the narrow pitch region is small.

Therefore, if the pitch between gate patterns **21**A and **21**B is not large enough, sidewall spacers **43**B and **44**C are formed in contact with each other as illustrated in FIG. **3**C in the present embodiment. That is, if the region between gate patterns **21**A and **21**B is a narrow pitch region, the sidewall spacers **44**B and **44**C in the narrow pitch region are formed in contact with each other. By forming the sidewall spacers **44**B and **44**C in the narrow pitch region so that the sidewall spacers **44**B and **44**C are in contact with each other, deep-SD impurity implantation into the narrow pitch region of the semiconductor substrate **2** may be reduced. As a result, degradation of the short-channel characteristics may be reduced.

If the pitch between gate patterns **21**A and **21**B is large enough as illustrated in FIG. **3**D, a deep-SD impurity may be implanted into the PMOS region of the semiconductor substrate **2** even if sidewall spacers **44**A and **44**B are formed.

In FIG. **4**A, horizontal axis shows overetching rate (%) of sidewall film **31**, and vertical axis shows resulting width of sidewall spacers **32** and **33**. In FIG. **4**A, the symbol ○ represents data on a wide pitch region and □ represents data on a narrow pitch region. The sidewall films **31** in the wide and narrow pitch regions were etched under the same conditions.

As illustrated in FIG. **4**A, under the same conditions, the resulting widths of the sidewall spacers **32** and **33** in the narrow pitch region is smaller than those of the sidewall spacers **32** and **33** in the wide pitch region.

In FIG. **4**B, horizontal axis shows overetching rate (%) of sidewall film **42**, and vertical axis shows resulting width of sidewall spacers **43** and **44**. In FIG. **4**B, the symbol ○ represents data on a wide pitch region and □ represents data on a narrow pitch region. The sidewall films **42** in the wide and narrow pitch regions were etched under the same conditions.

As illustrated in FIG. **4**B, under the same conditions, the resulting widths of the sidewall spacers **43** and **44** in the narrow pitch region is smaller than those of the sidewall spacers **43** and **44** in the wide pitch region.

FIGS. **5**A to **5**I illustrate a process for fabricating the semiconductor device continued from FIG. **1**Y. The photoresist **47** formed over the NMOS region of the semiconductor substrate **2** is removed by ashing or a wet process using an agent such as SPM. Then spike annealing is applied to the semiconductor substrate **2** in order to activate the impurity implanted in the NMOS and PMOS regions of the semiconductor substrate **2**. The spike annealing is performed at 1050° C., for example. In order to further activate the impurity implanted in the NMOS and PMOS regions of the semiconductor substrate **2** and to reduce abnormal diffusion of the impurity, flashlamp annealing or laser spike annealing may be applied at a temperature higher than or equal to 1150° C. for a millisecond time in addition.

The sidewall spacer **43** in the NMOS region of the semiconductor substrate **2**, the sidewall spacer **44** in the PMOS region of the semiconductor substrate **2**, and the native oxide film on the surface of the silicon substrate **2** are removed by a wet process using an HF solution. As illustrated in FIG. **5**A, a silicide **48** such as $NiSi_x$ is formed over the gate patterns **20** and **21**, the buffer region **35**, the deep-SD region **46**, and the epitaxial layer **41**. Before forming the silicide **48**, the sidewall spacers **43** and **44** are removed.

In order to increase the electron mobility in the NMOS, or as an etching stopper in formation of a contact hole, a tensile film **49** having a tensile stress is formed over the entire NMOS and PMOS regions of the semiconductor substrate **2**. For example, SiN film may be deposited over the semiconductor substrate **2** by PECVD to a thickness in the range from 30 nm to 100 nm to form the tensile film **49**.

A photoresist **50** is formed over the NMOS region of the semiconductor substrate **2** by photolithography. As illustrated in FIG. **5**B, the photoresist **50** is used as a mask to anisotropically etch the tensile film **49** in the PMOS region of the semiconductor substrate **2** by RIE to selectively remove the tensile film **49** from the PMOS region of the semiconductor substrate **2**. The photoresist **50** may be selectively formed over multiple NMOS regions of the semiconductor substrate **2**. With this, the tensile film **49** in the multiple NMOS regions of the semiconductor substrate **2** may be selectively removed.

The photoresist **50** formed over the NMOS region of the semiconductor substrate **2** is removed by ashing or a wet process using an agent such as SPM. In order to increase the hole mobility in the PMOS region, or as an etching stopper in formation of a contact hole, a compressive film **51** having a compressive stress is formed over the entire NMOS and PMOS regions of the semiconductor substrate **2**. For example, SiN film may be deposited over the semiconductor substrate **2** by PECVD to a thickness in the range from 30 nm to 100 nm to form the compressive film **51**.

A photoresist **52** is formed over the PMOS region of the semiconductor substrate **2** by photolithography. As illustrated in FIG. **5**C, the photoresist **52** is used as a mask to anisotropically etch the compressive film **51** in the NMOS region of the semiconductor substrate **2** by RIE to selectively remove the compressive film **51** from the NMOS region of the semiconductor substrate **2**. The photoresist **52** may be selectively formed over multiple PMOS regions of the semiconductor substrate **2**. With this, the compressive film **51** in the multiple PMOS regions of the semiconductor substrate **2** may be selectively removed.

As illustrated in FIG. **5**D, an interlayer insulating film **53** is formed over the tensile film **49** and the compressive film **51**. For example, SiO_2 film may be deposited over the tensile film **49** and the compressive film **51** by CVD from TEOS to a thickness in the range from 0.5 μm to 0.7 μm to form the interlayer insulating film **53**.

The interlayer insulating film **53** is planarized by CMP. A contact hole pattern is formed over the interlayer insulating film **53** by photolithography. As illustrated in FIG. **5**E, the interlayer insulating film **53** is etched by RIE to form contact holes **54** in the interlayer insulating film **53**.

A diffusion barrier having a multilayer structure of TiN and Ti is formed in the contact holes **54**. Then, the contact holes **54** are filled with W (tungsten) and W (tungsten) is deposited over the interlayer insulating film **53** by CVD, for example. The W over the interlayer insulating film **53** is polished by CMP. W is left only in the contact holes **54** to form W plugs **55** as illustrated in FIG. **5**F.

In order to form an interconnect trench for a first interconnect to be formed by a damascene process, a first interconnect interlayer insulating film **56** is formed over the interlayer insulating film **53** and the W plugs **55** as illustrated in FIG. **5**G. The first interconnect interlayer insulating film **56** is an oxide film or a low-dielectric-constant insulating film, for example. A wiring pattern is formed over the first interconnect interlayer insulating film **56** by photolithography.

As illustrated in FIG. **5**H, the wiring pattern formed over the first interconnect interlayer insulating film **56** is used as a mask to anisotropically etch the first interconnect interlayer insulating film **56** by RIE to form interconnect trenches **57**.

The interconnect trenches **57** are filled with a barrier metal and Cu (copper) and the barrier metal and Cu are deposited over the first interconnect interlayer insulating film **56**. As illustrated in FIG. **5**I, the barrier metal and Cu on the first

interconnect interlayer insulating film **56** is polished by CMP to form a copper interconnect **58**, which is a first interconnect.

For example, if the gate pitch of adjacent NMOS regions is in the range from 140 nm to 180 nm, the sidewall spacers **43** in the adjacent NMOS regions may be formed in contact with each other to reduce a deep-SD impurity from being implanted into the NMOS regions of the semiconductor substrate **2**. In this case, the sidewall spacers **43** in the adjacent NMOS regions with a gate pitch in the range from 140 nm to 180 nm may be formed in contact with each other by controlling the conditions under which the sidewall film **42** is formed. This applies to adjacent PMOS transistors as well.

Whether the space between gate patterns in adjacent NMOS regions is to be filled or not is determined based on the gate pitch of the NMOS regions. However, in practice, the gate height is also related and therefore whether the space between gates in adjacent NMOS regions is to be filled or not may be determined by the aspect ratio (AR) of the gate height to gate pitch. For example, in a narrow pitch region with an aspect ratio of 0.4 or less, the widths of sidewalls may be designed so that the space between the gates of adjacent NMOS regions is filled. In a narrow pitch region with an aspect ratio greater than 0.4, the width of side walls may be designed so that the space between gates of the adjacent NMOS regions is not filled. This applies to adjacent PMOS transistors as well.

The present embodiments have been described with respect to an example in which an n-type impurity is implanted in the gate polysilicon **9** in NMOS regions. However, the step of implanting an n-type impurity in the gate polysilicon **9** in NMOS regions may be omitted because the n-type impurity has been implanted in the gate pattern **20** in the step of implanting the deep-SD impurity in the NMOS regions of the semiconductor substrate **2**.

The present embodiments have been described with respect to an example in which a p-type impurity is implanted in the gate polysilicon **9** in PMOS regions. However, if the step of implanting a deep-SD impurity into the PMOS regions of the semiconductor substrate **2** is performed, the p-type impurity is also implanted in the gate pattern **21** and therefore the step of implanting the p-type impurity into the gate polysilicon **9** in the PMOS regions may be omitted.

The sidewall spacers **43** and **44** are removed after the impurity implanted in the semiconductor substrate **2** is activated by heat treatment in the present embodiments. The present invention is not limited to the present embodiments, the impurity implanted in the semiconductor substrate **2** may be activated by heat treatment after the sidewall spacers **43** and **44** are removed. Semiconductor devices and methods for fabricating the semiconductor devices according to the present embodiments include a semiconductor device having multilayer interconnections and a method for fabricating the semiconductor device.

All examples and conditional language recited herein are intended for pedagogical purposes to aid the reader in understanding the invention and the concepts contributed by the inventor to furthering the art, and are to be construed as being without limitation to such specifically recited examples and conditions, nor does the organization of such examples in the specification relate to a showing of the superiority and inferiority of the invention. Although the embodiments of the present inventions have been described in detail, it should be understood that the various changes, substitutions, and alterations could be made hereto without departing from the spirit and scope of the invention.

What is claimed is:

1. A method of manufacturing a semiconductor device comprising:

forming a first gate pattern and a second gate pattern adjacent to the first gate pattern in a first region of a semiconductor substrate;

forming a third gate pattern in a second region of the semiconductor substrate:

forming a first sidewall spacer on a sidewall of the first gate pattern, a second sidewall spacer on a sidewall of the second gate pattern, and a third sidewall spacer on a sidewall of the third gate pattern;

forming a first impurity region between the first gate pattern and the second gate pattern, a second impurity region opposite to the first impurity region across the first gate pattern, and a third impurity region opposite to the first impurity region across the second gate pattern, by implanting a first impurity into the first region of the semiconductor substrate using the first gate pattern, the first sidewall spacer, the second gate pattern, and the second sidewall spacer as a mask;

forming a fourth impurity region on both sides of the third gate pattern by implanting a second impurity into the second region of the semiconductor substrate using the third gate pattern and the third sidewall spacer as a mask;

etching the semiconductor substrate in the second region using the third gate pattern and the third sidewall spacer as a mask to form a trench;

forming a semiconductor layer in the trench;

after forming the semiconductor layer, depositing a first insulating film over the first region and the second region;

etching the first insulating film to form a fourth sidewall spacer on a side surface of the first sidewall spacer, a fifth sidewall spacer on a side surface of the second sidewall spacer, and a sixth sidewall spacer on a side surface of the third sidewall spacer in such a manner that the fourth sidewall spacer and the fifth sidewall spacer are in contact with each other between the first gate pattern and second gate pattern;

forming a fifth impurity region adjacent to the second impurity region and a sixth impurity region adjacent to the third impurity region by implanting a third impurity into the first region of the semiconductor substrate using the first gate pattern, the first sidewall spacer, the fourth sidewall spacer, the second gate pattern, the second sidewall spacer, and the fifth sidewall spacer as a mask, so that the fourth sidewall spacer and the fifth sidewall spacer which are in contact with each other block the third impurity to be implanted into the first impurity region between the first gate pattern and the second gate pattern;

forming a seventh impurity region on both sides of the third gate pattern by implanting a fourth impurity into the second region of the semiconductor substrate using the third gate pattern, the third sidewall spacer and sixth sidewall spacer as a mask; and

after implanting the third impurity and implanting the fourth impurity, removing the fourth sidewall spacer, the fifth sidewall spacer, and the sixth sidewall spacer.

2. The method according to claim **1**, further comprising:

after removing the fourth sidewall spacer, the fifth sidewall spacer, and the sixth sidewall spacer, forming a silicide in the first region and the second region of the semiconductor substrate.

3. The method according to claim **1**, wherein the semiconductor layer includes SiGe.

4. The method according to claim 3, wherein the first gate pattern and the second gate pattern are gate electrodes of an N-type MOS transistor, and the third gate pattern is a gate electrode of a P-type MOS transistor.

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